HAL RVD-1005 VISUAL DISPLAY UNIT

INSTRUCTION MANUAL

HAL COMMUNICATIONS CORP.
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URBANA, ILLINOIS 61801

QUALITY COMMUNICATIONS EQUIPMENT

HAL RVD-1005 VISUAL DISPLAY UNIT

TECHNICAL MANUAL

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WARRANTY

The HAL Communications RVD-1005 Visual Display Units is fully guaranteed against defects in material and workmanship for a period of one year. Should repair or replacement parts be required, notify HAL Communications Corp. promptly. The warranty period is measured from the date of the original invoice to the postmark date of your notification letter. Please do not return your unit to the factory for repair or adjustment until you have received a written return authorization.

HAL Communications assumes no responsibility for the repair or replacement of parts for units which have been damaged, abused, improperly installed, or modified and reserves the right to change the design of this visual display system without incurring obligation to incorporate such changes into existing units

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1. Introduction and Specifications

The HAL Communications RVD-1005 is a visual display unit designed for use in radioteletype systems. It is capable of decoding, storing, and displaying up to 1000 alphanumeric characters on the screen of a video monitor or converted television receiver.[1] When used with a suitable demodulator (terminal unit) such as the HAL ST-5 or ST-6, it provides instantaneous, silent reception of radioteletype signals.

A successor to HALs popular RVD-1002, the 1005 offers an improved display format, an automatic speed indicator, and input terminals for both loop and EIA-level inputs. Special circuitry has been added to prevent overprinting and the splitting of short words at the end of a line.

The RVD-1005 accepts serially transmitted character codes and generates the video signal required to display those characters on the monitor screen. The incoming characters are stored in a recirculating memory, which is used to refresh the display on every complete scan of the raster.

Display Characteristics

The 1000-character display "page" is divided into 25 horizontal lines of 40 characters each. Characters are produced by a pattern of bright dots on a dark field. The 35 dots in the matrix used to display each character are arranged in five vertical columns of seven dots each, as shown in Figure 1.1. The character height is equal to the space required for seven horizontal scan lines. The width is approximately five sevenths of the height. The actual size of the displayed characters depends, of course, on the size of the monitor screen. Complete display specifications are given in Table 1.1.

The first incoming characters appear on the bottom line of the display. When that line is full, all characters in it shift up one line, leaving the bottom line blank and ready to receive new characters. This line feed process recurs each time the bottom line is filled or when a line feed character is received. To prevent the splitting of short words at the end of a line, a line feed occurs automatically if a space is received after the 34th character in a line.[2] The characters which follow the space appear at the left margin of the next line. When all 25 lines have been used, the next line feed causes the top line to be deleted.

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[1] The video monitor is not supplied with the RVD-1005. An optional monitor is available. Section 5 provides instructions for modifying a television receiver to serve as a monitor.

[2] In early production units with serial numbers less than 220, the line feed occurs if a space is received after the 36th character.

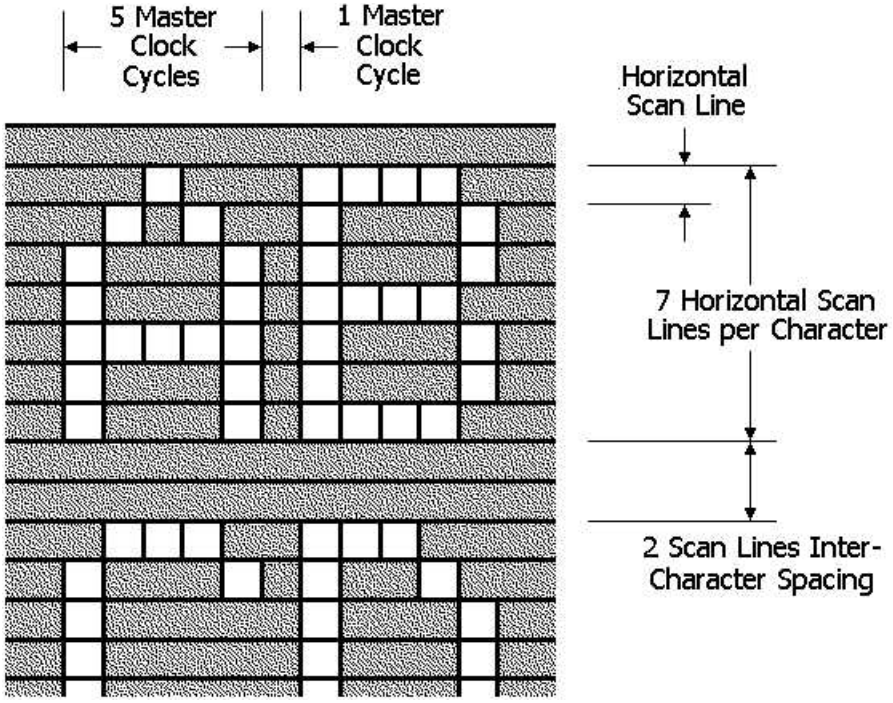


Figure 1.1 Character Display Format

TABLE 1.1 DISPLAY SPECIFICATIONS

Character format	5 × 7 dot matrix
Line format	40 characters/line
Page format	25 lines/page
Character width-to-space ratio	5:2
Character-plus-space time[3]	875 nanoseconds
Line height-to-space ratio	7:2
Horizontal scan lines per character line	7
Horizontal scan lines per intercharacter space	2
Horizontal line display percent[4]	83 percent
Vertical field display percent[5]	78 percent

[3] Defined as the time required during a horizontal scan to display one character plus an intercharacter space.

[4] Defined as the percentage of the horizontal line used in displaying 40 characters and the spaces between them.

[5] Defined as the percentage of the vertical field used in displaying 25 character lines and the interline spaces.

Input Characteristics

The display unit inputs accept serially transmitted, five-level, Baudotcoded characters, the standard for radioteletype and many other types of data transmission. The unit operates at all standard speeds – 60, 66, 75, and 100 words per minute.

Two separate input jacks are provided. One accepts voltage inputs and is designed to be compatible with EIA standard voltage levels. A current input is also provided and can be used to connect the system in series with the station loop circuit. Complete input specifications appear in Table 1.2.

Figure 1.2 shows the format of the input code. The code for a particular character consists of a start pulse, five data pulses, and a stop pulse. Each pulse may represent either a "mark" or a "space". In terms of the voltage input, space pulses are positive; mark pulses are negative. For the loop circuit input, mark pulses are represented by the flow of current. During space pulses, the current is interrupted.

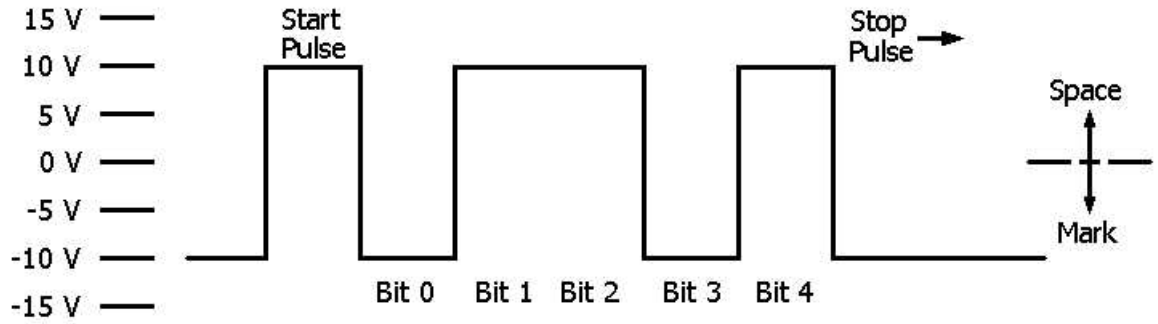


Figure 1.2 Format of Typical Input Character

The start pulse for any character is a space. Data pulses 0 through 4 follow the start pulse and may be either marks or spaces, depending on the character being received. The stop pulse is a mark. All pulses are of equal length except the stop pulse, which may be longer than the others. The pulse length varies with the operating speed, as indicated in Table 1.2.

As Figure 1.3 illustrates, the input mark and space pulses must fall within a certain voltage or current range to produce valid copy. For the voltage input, space pulses must be in the range from +5 to +15 volts. Mark pulses must lie between -5 and -15 volts. When the current input is used, the loop current must be in the range from 18 to 120 mA for mark pulses and less than 2 mA for spaces. Pulses which fall in the forbidden current or voltage ranges may cause uncertainty or errors in the display.

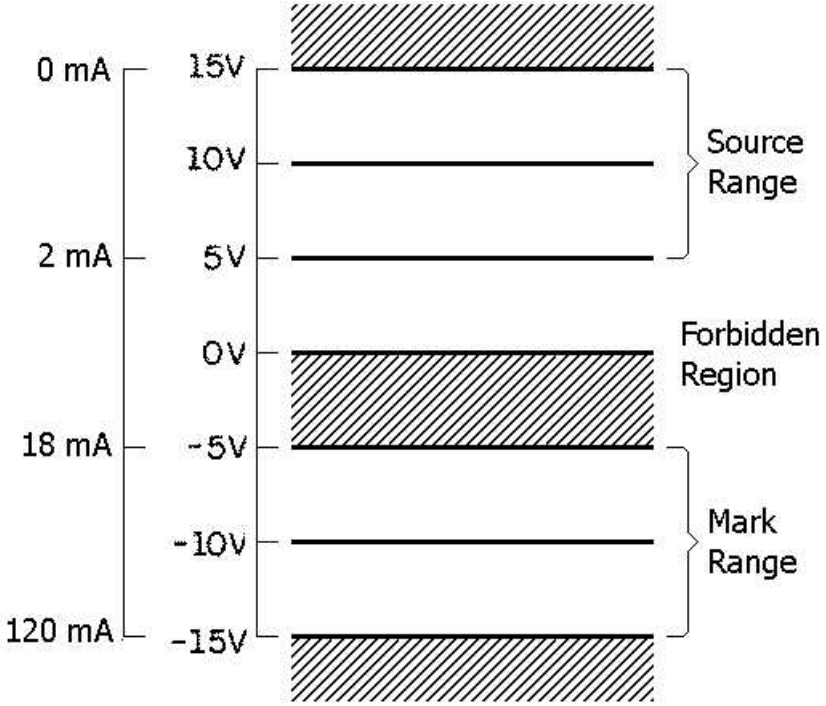


Figure 1.3 Input Limits

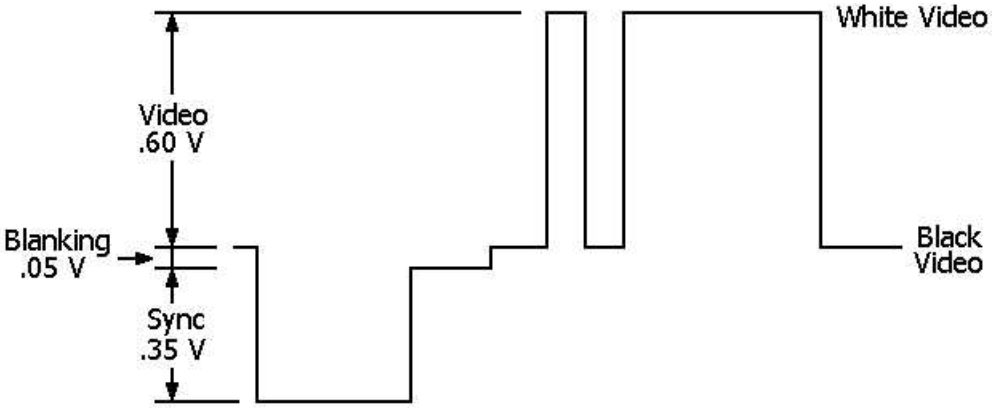


Figure 1.4 Video Output Format

TABLE 1.2 INPUT SPECIFICATIONS

Input data form:	Serial
Word format	
Pulse 1:	Start pulse
Pulse 2:	Data pulse 0
Pulse 3:	Data pulse 1
Pulse 4:	Data pulse 2
Pulse 5:	Data pulse 3
Pulse 6:	Data pulse 4
Pulse 7:	Stop pulse
Select pulse length	
60 WPM:	22 milliseconds
66 WPM:	20 milliseconds
75 WPM:	17.57 milliseconds
100 WPM:	13.47 milliseconds
Start pulse length:	Same as select pulse
Data pulse length:	Same as select pulse
Stop pulse length:	Greater than or equal to select pulse
Voltage input characteristics	
Mark voltage:	-5 to -15 volts
Space voltage:	+5 to + 15 volts
Input impedance:	120 ohms or greater
Loop (current) input	
Mark current:	18 to 120 mA
Space current:	2 mA or less
Input impedance:	20 ohms or less
Isolation, loop to case:	10 megohms or greater

Output Characteristics

The output video signal is compatible with EIA RS-170, 525-line-per-frame television systems, standard in the United States. Table 1.3 lists the video output specifications; the waveform is shown in Figure 1.4. Detailed instructions for connecting the RVD-1005 video output to a television receiver are given in Section 5.

Construction and Physical Specifications

The RVD-1005 circuitry is constructed on two printed circuit boards. The logic and signal-processing circuitry occupies the larger of these boards. The power supply components are mounted on the smaller one. They are housed in an attractive two-tone gray cabinet. A rack-mounting model, the RVD-1005R, is designed for installation in a standard 19-inch relay rack. Size, weight, temperature, and input power specifications are given in Table 1.4.

Accessories

The RVD-1005 is supplied with the following accessories:

Four-foot video cable with male BNC connector at each end
Two four-foot two-conductor shielded cables
Two input connector shells (male)
12 connector pins (female)
One manual

TABLE 1.3 VIDEO SPECIFICATIONS

Lines per field:	262.5
Fields per frame:	2
Lines per frame:	525
Line rate:	15.750 kHz
Field rate:[6]	60 Hz
Timing tolerance:	±0.1 %
Synchronization voltage:	0.35 volt peak-to-peak
Synchronization polarity:	negative
Video voltage:[7]	0.60 volt peak-to-peak
Composite video signal voltage:	1.0 volt peak-to-peak
Voltage tolerance:	±10 % with specified load
Peak video bandwidth:[8]	3.1 MHz
Load impedance:	75 ohms ±5 %

TABLE 1.4 GENERAL SPECIFICATIONS

Size:	RVD-1005	3.5" H, 17" W, 9" D (8,9 × 43,2 × 22,9 cm)
	RVD-1005R	3.5" H, 19" W, 9" D (8,9 × 48,3 × 22,9 cm)
Weight:	7.5 pounds (3,4 kilograms)	
Shipping weight:	14 pounds (6,4 kilograms)	
Operating temperature:	65 to 80 °F (18.3 to 26.7 °C)	
Power requirements:	105 to 125 VAC, 50 to 60 Hz, 25 watts 210 to 250 VAC, 50 to 60 Hz, 25 watts	

[6] Fields are automatically interlaced.
[7] Figure 1.4 shows the proper video output waveform.
[8] Defined as the frequency above which all energy could be eliminated with no degradation of picture quality. Readability decreases noticeably when energy below 3.1 MHz is eliminated.

2. Installation and Operating Instructions

Installation

The RVD-1005 is very simple to install. The first step is to connect the video output to an external video monitor. A four-foot cable with BNC connectors at each end is supplied for this purpose. Connect one end of the cable to the rear-panel jack labeled VIDEO OUTPUT, as shown in Figure 2.1. Connect the other end to the video input jack of your monitor.

NOTE: The video output line must be terminated by a 75-ohm impedance. Check the monitor specifications to determine whether its input represents a 75-ohm load. The load need not provide a DC return path.

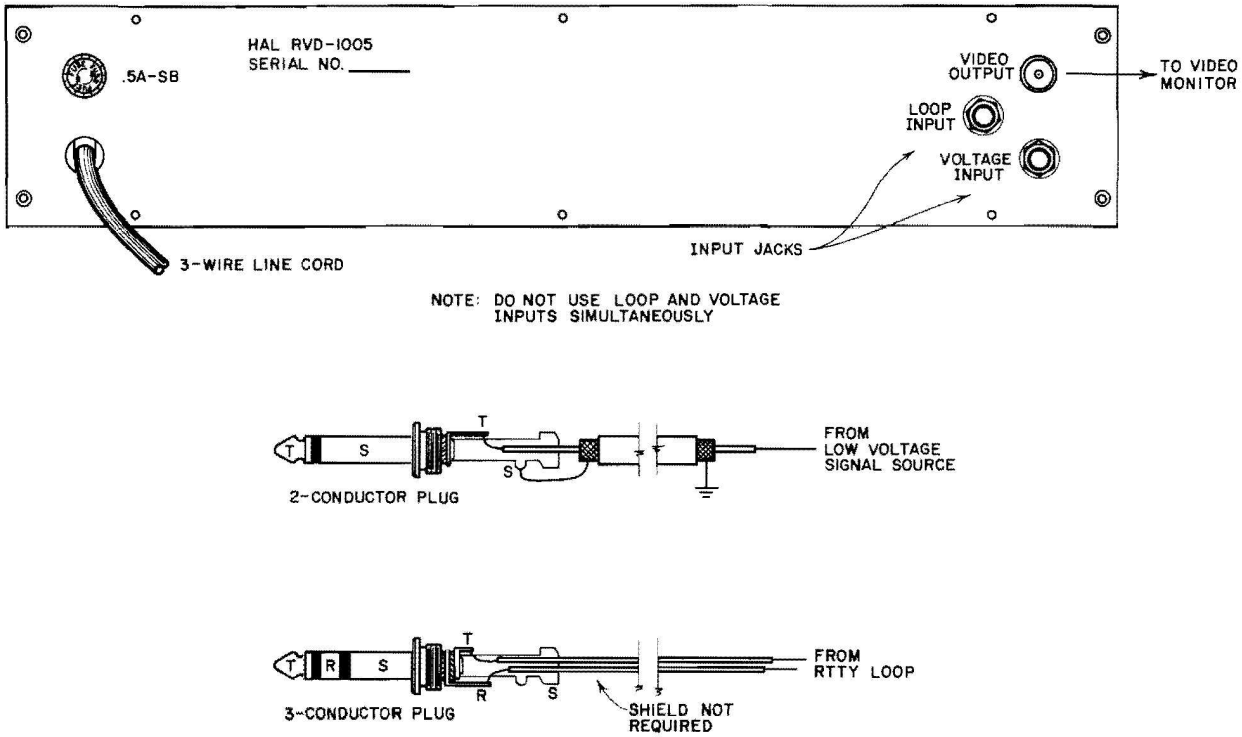
You may easily modify a standard television receiver for use as a video monitor. Full details are given in Section S of this manual. DO NOT use a television set in which one side of the AC power line is connected directly to the chassis or to the ground return for the circuitry unless you supply AC power to the set from a reliable isolation transformer.

Two inputs are provided. One is a voltage input which may be driven by an output from your terminal unit (demodulator), provided that the mark and space voltage levels fall within the range indicated in Figure 1.3. If you prefer, or if an output of the required voltage level is not available on your terminal unit, you may connect the RVD-1005 in series with other equipment in your DC printer loop circuit by using the LOOP input connections. Break the station loop and connect the two cable conductors in series with the other equipment. The polarity is not important.

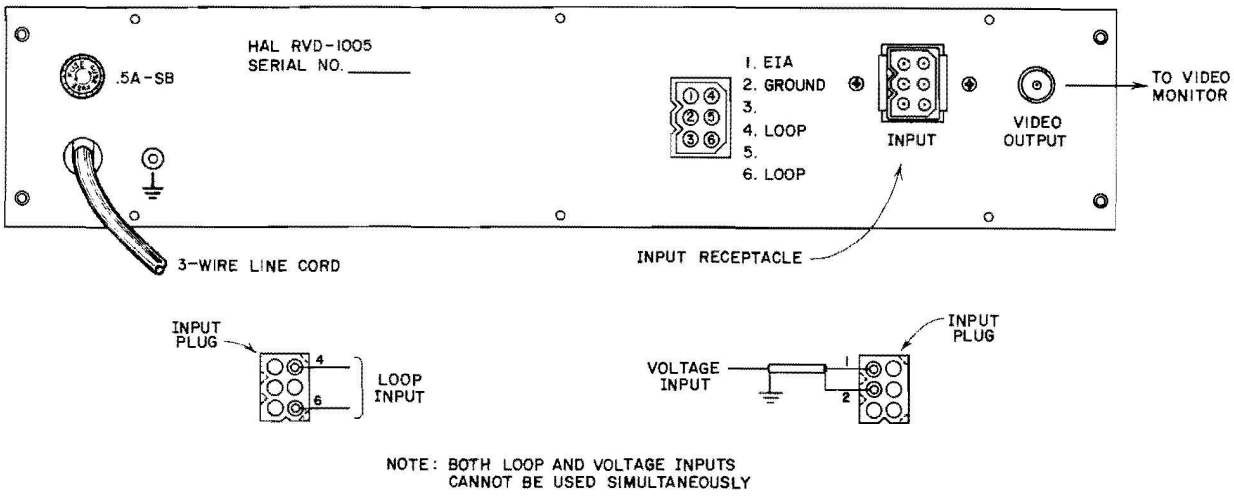
If you plan to drive the RVD-1005 input from a HAL ST-S or ST-6 terminal unit, the voltage input may be connected directly to the FSK jack of the terminal unit. For other demodulators, check the voltage levels carefully before connecting the signal to the visual display unit input.

NOTE: The two inputs (VOLTAGE INPUT and LOOP) may not be used simultaneously. Make connections to one or the other but not both.

A six-pin connector on the rear panel of the RVD-1005 can be wired for either voltage or current (loop) inputs. The correct connections are shown in Figure 2.1. Attach the pins to the wires as shown in Figure 2.2 and insert the pins in the locations indicated in Figure 2.1. Once inserted in the shell, the pins are not easily removed. Sufficient pins and two plug shells are provided so that cables for both loop and voltage inputs can be prepared.



a. RVD-1005 Serial Number Less Than 346



b. RVD-1005 Serial Number 346 and Higher

Figure 2.1 Rear Panel Connections

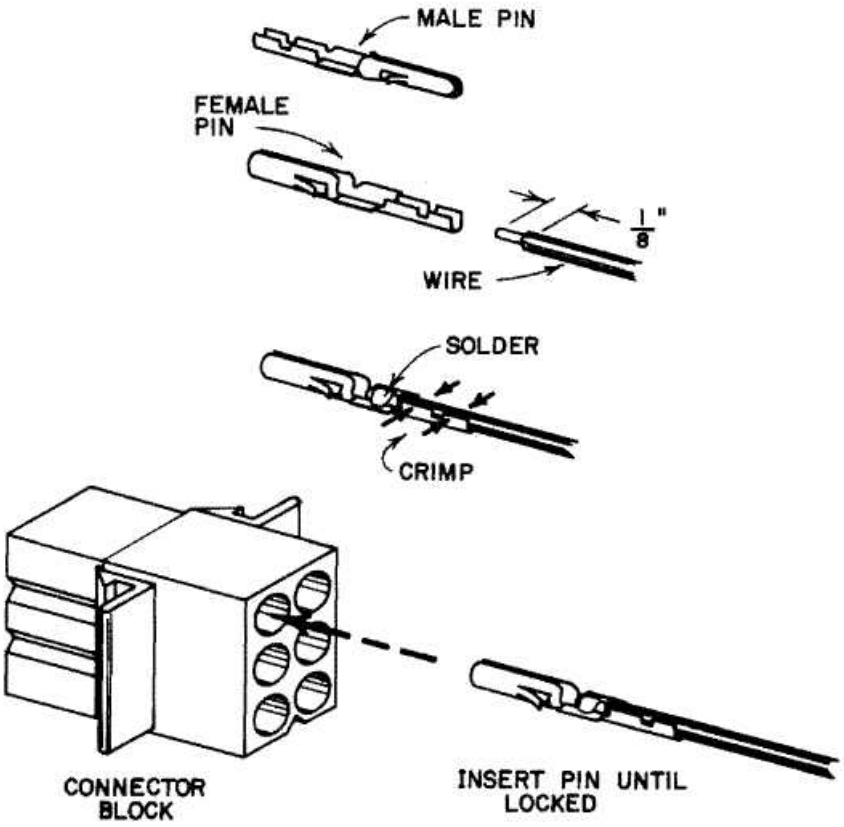


Figure 2.2 Preparation of Input Connector

Two slightly different ways in which the RVD-1005 can be connected to a teletype system are shown in Figures 2.3 and 2.4. The use of the FSK data output connection of the ST-6 (or ST-S) to drive the RVD is shown in Figure 2.3. As noted, shielded cables should be used between the ST-6 and the RVD as well as for the video connection, scope connection, and audio input and output connections. The connections to the DKB-2010 and TTY machine can be made with twin parallel-conductor cable ("zip-cord") or other two-conductor cable. The shielded cables should be as short as possible for a given installation but may be as long as six feet or more if necessary. Longer cable lengths may result in problems with RF interference or ground loops. In all cases, the cabinets of all parts of the system should be positively connected together with 18 gauge wire or ¼" wide shield braid to assure good ground connections. DO NOT rely upon the power cord safety grounds or the shield of shielded signal cables to provide a RF ground-return-path. Figure 2.4 illustrates how the RVD-1005 may be connected in a standard 60 ma series TTY loop circuit. None of the loop connections need be shielded, but all equipment cabinets should be bonded together. The ST-6 (or ST-S) may also be connected in this manner, if desired. Be sure that connections are made to the proper input pins of the RVD input connector and that the voltages and currents are compatible with the limits shown in Figure 1.3 and Table 1.2.

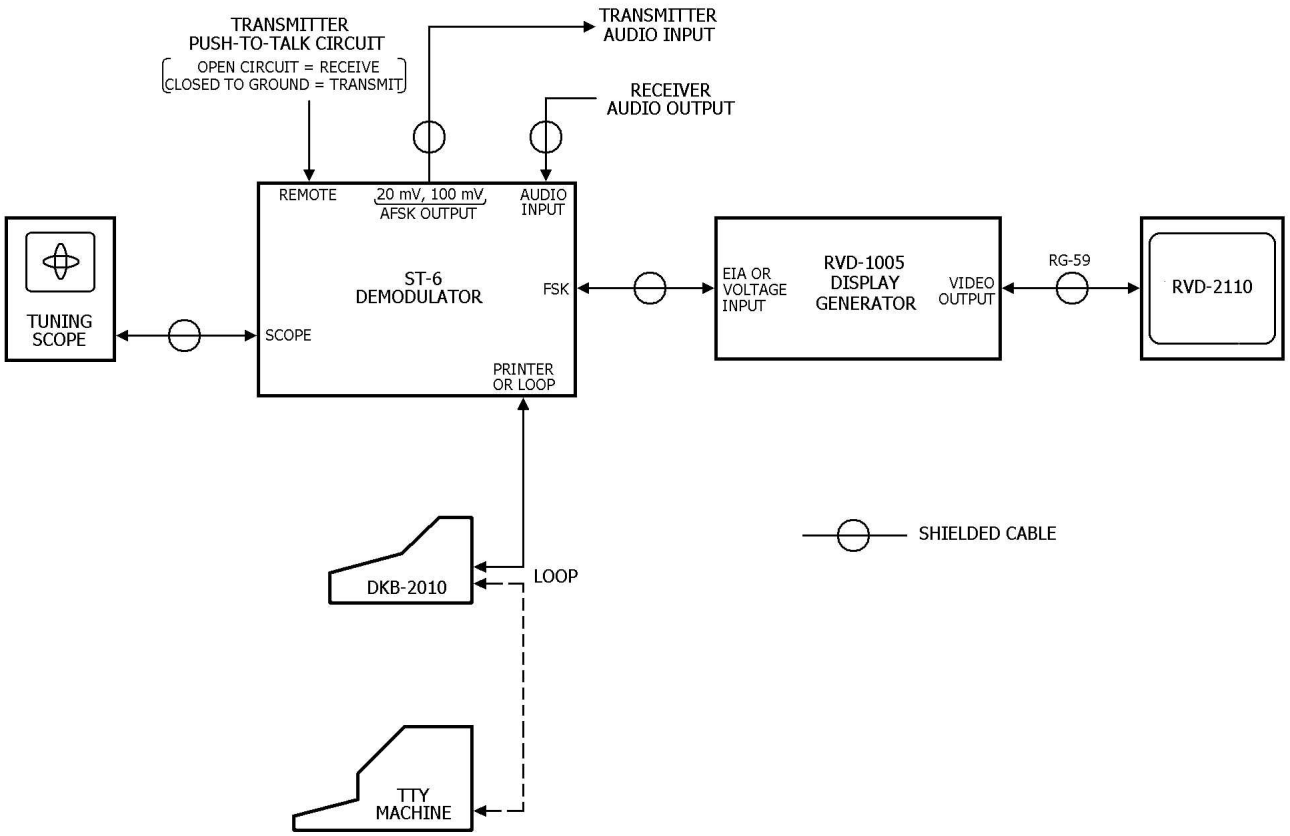


Figure 2.3 Connection of the RVD with the ST-6

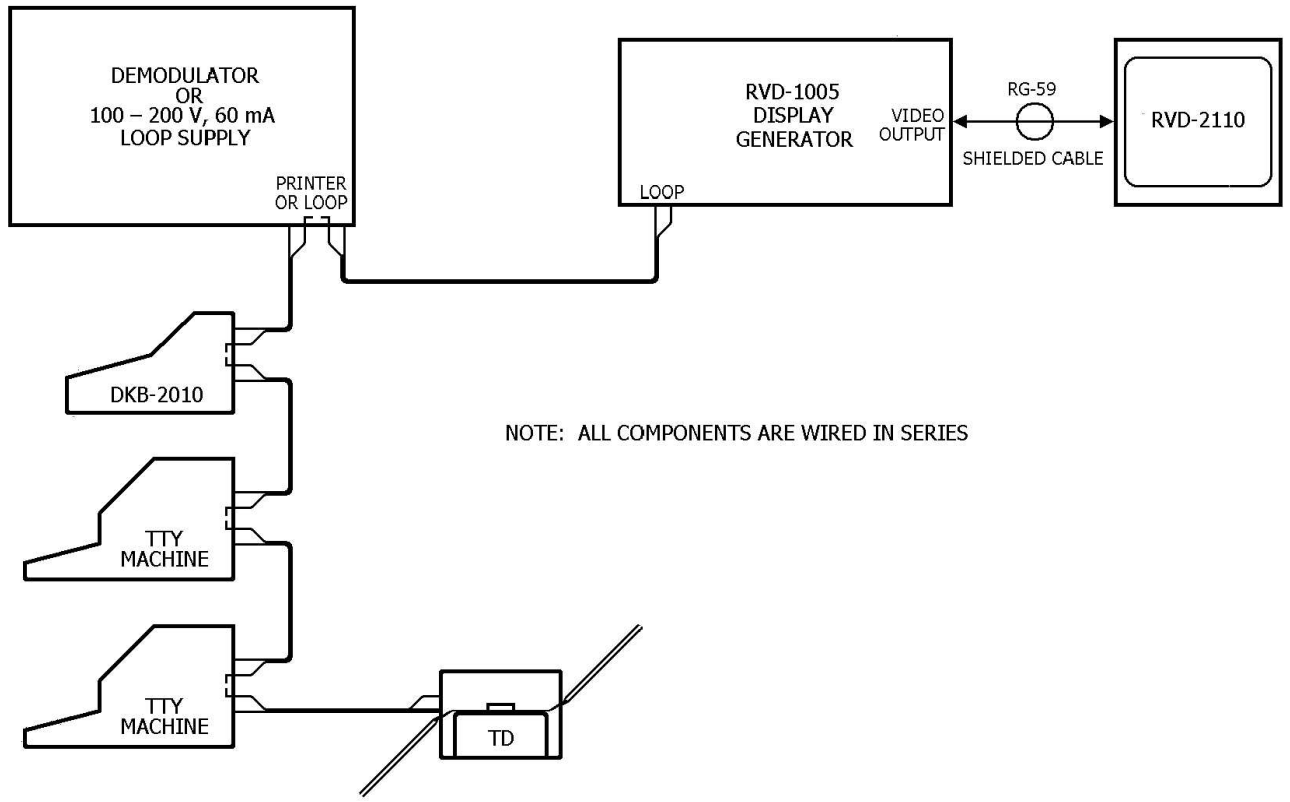


Figure 2.4 Connection of the RVD in a 60 mA Loop Circuit

Check the input voltage specification for your unit. It is designed for 115 volt, 50 to 60 Hz operation unless otherwise requested on your order. Units equipped for operation from nominal 230 volt, 50 to 60 Hz power sources are identified by a label on the rear panel and a tag on the power cord.

Connect the AC cord to a power source of the proper voltage and frequency. Use only a three-wire grounding AC outlet to protect the operator from electrical shock and to minimize interference from stray RF fields.

When mounting your unit, check that the ventilation holes in the top and bottom covers are not obstructed. Avoid mounting it above units which generate heat.

Operation

The RVD-1005 is as simple to operate as it is to install. The eight pushbuttons on the front panel, shown in Figure 2.5, control all functions.

Provide an input signal by tuning to a RTTY station. Choose a signal that is relatively noise free and, if possible, of known speed. Check that the terminal unit is demodulating the signal properly. If you have connected your display unit into the station loop circuit rather than to the terminal unit, you may prefer to generate an input signal by typing on your keyboard or by running a paper tape on a tape reader connected into the loop.

Switch on the AC power to the video monitor or television receiver. Press any of the speed selector buttons to switch the visual display system on. With the test signal applied, observe the speed indicator lights located directly above the speed selector buttons. The one corresponding to the speed (in words per minute) of the input signal should light. Press the speed button directly below the light to set the RVD-1005 to the correct operating speed. Characters should start to appear on the monitor screen.

The speed may be changed at any time by pressing one of the other speed selector buttons. Note that the speed lights simply indicate the speed of the incoming signal; they do not set the unit's operating speed. That function is always performed manually by the operator, using the speed selector buttons.

The speed indicator lights give an *estimate* of the speed of the received signal. They may provide an incorrect indication if the input signal is noisy, if its speed is significantly different from the display unit's four standard operating speeds, or if the received signal has significant bias distortion (difference between the durations of mark and space pulses).

The UNSHIFT ON SPACE button, located to the left of the four speed selectors, activates the automatic letters-shift circuitry, which causes the display to return to letters case every time a space character is received. This feature prevents the system from erroneously displaying figures-case characters instead of letters if a letters-shift command is not received at the proper time. Press the button once to enable this feature; press it again to return to normal operation.

If you wish to manually return the system to letters case, press the MANUAL LTRS button momentarily. A letters-shift command will be produced, shifting the display to letters case and overriding any case control characters received while the button is pressed.

Similarly, the MANUAL LF button produces a linefeed command when it is pressed, causing all characters in the display to jump up one line and leaving the bottom line blank. The button overrides the input signal while it is depressed. Whenever a linefeed occurs, whether it is received in the input character stream or produced manually by pressing the button, a carriage return automatically occurs so that the next character will appear at the left margin.

Whenever a 40-character line has been filled, the unit causes a linefeed and carriage return to occur, so that the next character received will appear at the left margin of a new line. In addition, the linefeed and carriage return are automatically produced if a space is received after the 34th character in a line. This feature prevents the splitting of words which start near the end of a line.

When you have finished using the display unit, remove AC power by pressing the POWER button located to the right of the speed selectors.

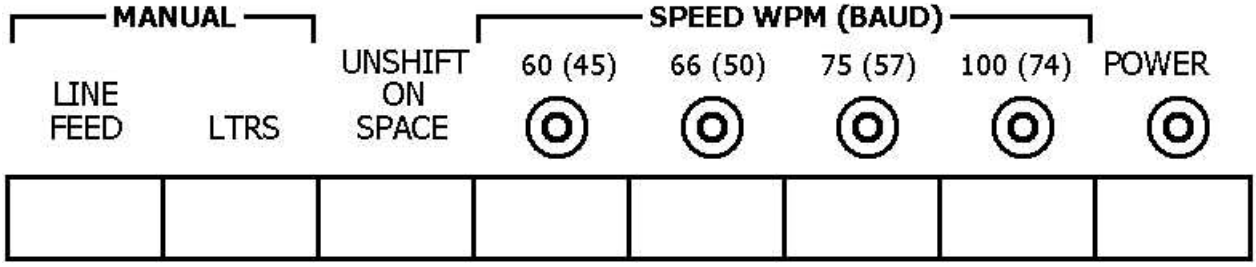


Figure 2.5 Front Panel Controls

3. Theory of Operation

Basic Operating Principles

The RVD-1005 circuitry is composed of two main parts: (1) the input section, and (2) the memory and display section. A block diagram is shown in Figure 3.1. The input section accepts each character in sequence from the local loop or terminal unit, converts it from serial to parallel form and then from Baudot to a modified ASCII[9] code, checks it to determine whether it is a printing character or a control code (such as a line feed or carriage return), and stores it until the main memory is ready to accept it.

The memory and display section stores the incoming characters and maintains the display by continuously reading out the memory contents, generating the dot pattern required for each character, and producing the composite video signal fed to the monitor.

Teleprinter Code

In the standard Baudot code used in five-level teleprinter systems, each character is made up of seven sequential "select" pulses, as shown in Figure 3.2. Pulses may have either of two states; in the "mark" state, current flows in the printer loop, while in the "space" state it does not. The rest condition, when no characters are being transmitted, is always a mark.

In any character the first pulse, called the start pulse, is a space; it prepares the printer to accept the six succeeding pulses of that character. The five pulses which follow define the individual character. There is a unique pattern of these pulses for each character. The last pulse, called the stop pulse, is always a mark. It allows the printer to recover and prepare for the next character. All pulses are of equal length except for the stop pulse, which may be longer. The pulse length decreases with increased operating speed, as indicated in Table 1.2.

[9] ASCII denotes the American Standard Code for Information Interchange, widely used in data processing systems. Table 3.1 lists the Baudot codes and their ASCII equivalents for each character.

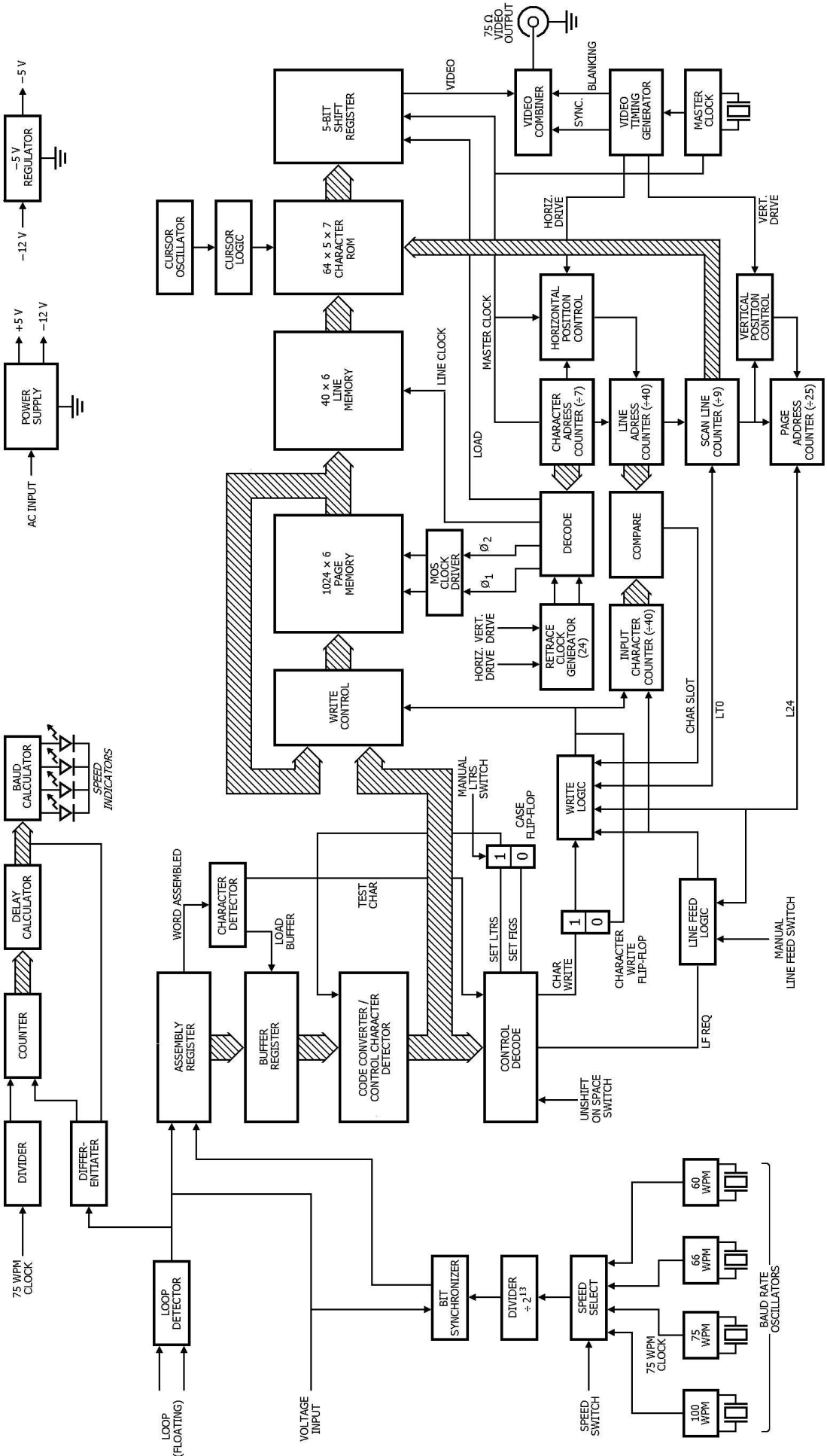


Figure 3.1 RVD-1005 Block Diagram

Character[11]	Baudot Code		ASCII Code[10]	
	Bit Number[12] 5 4 3 2 1	Case[13]	Bit Number 6 5 4 3 2 1	
A	0 0 0 1 1	L	0 0 0 0 0 1	
B	1 1 0 0 1	L	0 0 0 0 1 0	
C	0 1 1 1 0	L	0 0 0 0 1 1	
D	0 1 0 0 1	L	0 0 0 1 0 0	
E	0 0 0 0 1	L	0 0 0 1 0 1	
F	0 1 1 0 1	L	0 0 0 1 1 0	
G	1 1 0 1 0	L	0 0 0 1 1 1	
H	1 0 1 0 0	L	0 0 1 0 0 0	
I	0 0 1 1 0	L	0 0 1 0 0 1	
J	0 1 0 1 1	L	0 0 1 0 1 0	
K	0 1 1 1 1	L	0 0 1 0 1 1	
L	1 0 0 1 0	L	0 0 1 1 0 0	
M	1 1 1 0 0	L	0 0 1 1 0 1	
N	0 1 1 0 0	L	0 0 1 1 1 0	
O	1 1 0 0 0	L	0 0 1 1 1 1	
P	1 0 1 1 0	L	0 1 0 0 0 0	
Q	1 0 1 1 1	L	0 1 0 0 0 1	
R	0 1 0 1 0	L	0 1 0 0 1 0	
S	0 0 1 0 1	L	0 1 0 0 1 1	
T	1 0 0 0 0	L	0 1 0 1 0 0	
U	0 0 1 1 1	L	0 1 0 1 0 1	
V	1 1 1 1 0	L	0 1 0 1 1 0	
W	1 0 0 1 1	L	0 1 0 1 1 1	
X	1 1 1 0 1	L	0 1 1 0 0 0	
Y	1 0 1 0 1	L	0 1 1 0 0 1	
Z	1 0 0 0 1	L	0 1 1 0 1 0	
0	1 0 1 1 0	F	1 1 0 0 0 0	
1	1 0 1 1 1	F	1 1 0 0 0 1	
2	1 0 0 1 1	F	1 1 0 0 1 0	
3	0 0 0 0 1	F	1 1 0 0 1 1	
4	0 1 0 1 0	F	1 1 0 1 0 0	
5	1 0 0 0 0	F	1 1 0 1 0 1	
6	1 0 1 0 1	F	1 1 0 1 1 0	
7	0 0 1 1 1	F	1 1 0 1 1 1	
8	0 0 1 1 0	F	1 1 1 0 0 0	
9	1 1 0 0 0	F	1 1 1 0 0 1	
-	0 0 0 1 1	F	1 0 1 1 0 1	
$	0 1 0 0 1	F	1 0 0 1 0 0	
'	0 1 0 1 1	F	1 0 0 1 1 1	
,	0 1 1 0 0	F	1 0 1 1 0 0	
!	0 1 1 0 1	F	1 0 0 0 0 1	
:	0 1 1 1 0	F	1 1 1 0 1 0	
(	0 1 1 1 1	F	1 0 1 0 0 0	
"	1 0 0 0 1	F	1 0 0 0 1 0	
)	1 0 0 1 0	F	1 0 1 0 0 1	
#	1 0 1 0 0	F	1 0 0 0 1 1	
?	1 1 0 0 1	F	1 1 1 1 1 1	
&	1 1 0 1 0	F	1 0 0 1 1 0	
.	1 1 1 0 0	F	1 0 1 1 1 0	
/	1 1 1 0 1	F	1 0 1 1 1 1	
;	1 1 1 1 0	F	1 1 1 0 1 1	
BELL[14]	0 0 1 0 1	F	1 0 1 0 1 0	
BLANK[15]	0 0 0 0 0	L, F	0 0 1 0 1 1	
LF[15]	0 0 0 1 0	L, F	0 0 1 0 1 0	
CR[15]	0 1 0 0 0	L, F	0 0 1 1 0 1	
FIGS[15]	1 1 0 1 1	L, F	1 1 1 1 1 0	
LTRS[15]	1 1 1 1 1	L, F	1 1 1 1 0 0	
SPACE	0 0 1 0 0	L, F	1 0 0 0 0 0	

Table 3.1 Baudot and ASCII Codes

10 The six least significant bits are used for character recognition in the RVD-1005A. The seventh bit is used to indicate a space code for the unshift-on-space function and the eighth bit indicates control characters. In all cases, bits 1 through 5 are inverted in the RVD so that the space code generated is 1111 1111, allowing insertion of spaces for the line feed function. The logic levels are negative true; that is, a "0" is represented by a voltage level between +2.4 and +5.0 volts, a "1" by a level between 0 and +0.8 volts.

11 LF denotes line feed. CR denotes carriage return.

12 Bit number 1, the least signification bit, is transmitted first in the sequence of pulses. A "1" denotes a mark pulse; a "0" denotes a space.

13 L denotes letters (LTRS) case; F denotes figures (FIGS) case.

14 A "*" is printed on the screen for the BELL function.

15 The ROM does not generate true ASCII code for these control functions; only unique codes that can be recognized internally by the RVD input section.

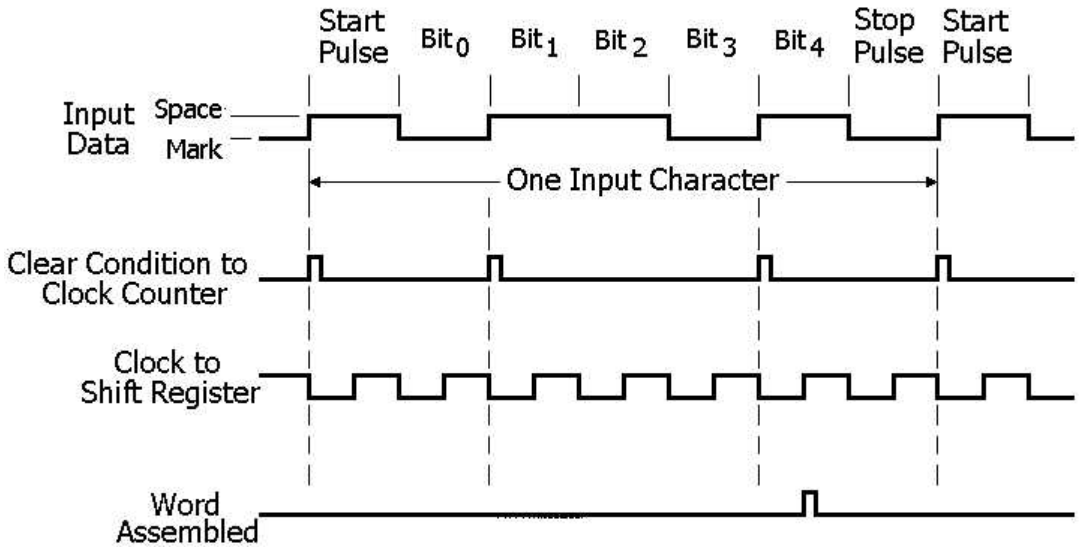


Figure 3.2 Input Character Waveform

INPUT SECTION

The input section accepts the incoming pulses for each character and stores the first six pulses (the start pulse and the five that define the character) in a shift register. The pulses, or "bits", which have been received in serial form – that is sequentially – are then all available simultaneously at the outputs of the shift register's six stages. That is, they have been converted to parallel form, or "assembled."

The five character-defining bits from the register outputs are fed to a buffer storage register and then to the address inputs of two read-only memories (ROMs) which convert the bit pattern to the standard ASCII code for the character. This ASCII code appears at the ROM outputs, ready for transfer to the page memory circuits in the memory and display section at the appropriate time during the memory cycle.

The input section operates independently from the memory and display section, interacting with it only when a character has been assembled and is ready to be transferred. The input section comprises these circuit functions:

1. Input timing chain (oscillators, speed selector, and divider);
2. Bit synchronizer;
3. Assembly register and character detector;
4. Buffer register;
5. Baudot-to-ASCII ROM code convertors;
6. Control decoder and case flip-flop;
7. Write command flip-flop;
8. Baud rate estimator.

Input Timing Chain

The operation of the input circuitry is synchronized with the speed of the incoming teletype signal by the input timing circuitry, shown in Figure 6.6. Four oscillators, one for each of the unit's four operating speeds, are provided. Each runs at a speed 2^{17} times the baud rate of the corresponding operating speed.

The unit's operating speed is determined by depressing one of four switches, activating the appropriate oscillator. The oscillator output is divided by a factor of 2^{13} (8,192) in a string of binary dividers to drive the input clock bus. The speeds and the corresponding frequencies are given in the following table.

Table 3.2 Input Timing Frequencies

Speed (words per minute)	Baud Rate	Select Pulse Length (msec)	Oscillator Frequency (MHz ±0.1 %)
60	45.45	22	5.9578
66	50.0	20	6.5536
75	56.9	17.57	7.4599
100	74.2	13.47	9.7306

Input Conditioning Circuitry

For voltage inputs, no signal conditioning is necessary. The input data signal from the RTTY demodulator is coupled directly to the *input data* line, which drives the first flip-flop of the bit synchronizer (IC-21). If, however, the current input is used to connect the visual display unit into the station loop circuit, it is necessary to convert the current to a voltage signal of the appropriate level. As shown in Figure 6.6, the current passes through a bridge rectifier which makes the input circuit insensitive to the polarity of current flow through the external loop circuit. The rectifier drives a light-emitting diode in an optical isolator. The diode's light output is detected by a light-sensitive transistor which forms part of the isolator. The desired voltage output is taken from the collector of the transistor to drive the *input data* line.

Bit Synchronizer, Assembly Register, and Buffer Register

The input signal is fed to the inputs of the assembly register and the bit synchronizer (consisting of ICs 20 and 21), as shown in Figure 6.5. The divide-by-16 counter is driven by the input clock signal, which supplies 16 clock pulses during the duration of each select pulse at the operating speed chosen. When the circuit is inactive (when no characters are being received and the input is resting in the mark state), the divide-by-16 counter is allowed to free run. When a space pulse is received, however, indicating the beginning of a character, the mark-to-space transition resets the counter to zero on the next clock pulse.

Eight clock pulses later (in the middle of the select pulse), the output (D) stage of the counter switches from the 0 to the 1 state, shifting the assembly register one stage. The counter continues its cycle, shifting the register once every 16 clock pulses until a new mark-to-space transition is received. Thus, each select pulse is sampled in the middle of its duration and entered in the register, and the register is resynchronized at the beginning of each character and also at every mark-to-space transition within a character.

The character detector determines when the start pulse has reached the last stage of the assembly register. At that point, the six stages of the register contain the start bit and all five of the select bits which define the character. The character detector then generates a command which allows these bits to enter the buffer register, where they are stored while the character is transferred to the page memory. At the same time, the assembly register is reset and is then ready to receive the next incoming character.

Code Convertor and Control Character Detector

The outputs of the buffer register carry the stored character code to the inputs of the ROM code convertor and control character detector. The Baudot bit pattern for each character addresses a unique memory location in the code convertor. Each memory location stores the ASCII code equivalent of the Baudot code which constitutes that location's address. Thus, the ASCII code for the character appears at the ROM output.

As may be seen in the schematic diagram (Figure 6.6), the code convertor actually consists of two ROMs with inputs and outputs tied in parallel. One ROM stores the ASCII codes for letters-

case Baudot characters; the other stores the codes for figures-case characters. Only one ROM is active at any time. The one chosen is determined by the state of the case flip-flop. In normal letters-case operation, the case flip-flop is in the set condition. Its output activates the letters ROM; the figures ROM is disabled. When a figures-shift character is received, the flip-flop changes states, activating the figures ROM and disabling the letters ROM. Thus, the correct ASCII code is produced for any character, whether in figures or letters case. The state of the case flip-flop can also be changed manually by the "manual letters" pushbutton or by the "unshift-on-space" feature (if activated), which returns the unit to letters case whenever a space is received.

There are five control characters in the normal Baudot character set: line feed (LF), carriage return (CR), letters shift (LTRS), figures shift (FIGS) and blank. These characters do not print on the screen, so they need not be entered in the page memory. The control decoder section contains circuitry which recognizes these control characters and instructs the logic circuit how to handle them.

The ROM code convertors are programmed so that the seventh bit is activated only when one of these control characters is received. This seventh bit is used to prevent the transfer of these characters to the page memory.

Logic gates decode the letters-and figures-shift characters and drive the case flip-flop. As described above, the state of this flip-flop determines which of the two code convertor ROMs is activated.

In the standard RVD-1005, the carriage return function is generated in the memory and display section, since the length of the display line (40 characters) does not correspond to the standard 72-character RTTY line. Incoming carriage returns are therefore ignored. Each time a line feed occurs, the next incoming character is automatically written in the first position of the new line at the left margin.

Line feeds are decoded and drive the *line feed request (LF REQ*) bus, signaling the line feed logic in the memory and display section to initiate a new display line.

Space characters are also detected, even though they do appear on the display. If a space occurs after the 34th character in a line, as indicated by the state of the input character counter in the memory and display section, a logic circuit generates a line feed command so that the next character will begin a new display line.

Once an incoming character has been assembled, stored in the buffer register, and converted to ASCII code, it is ready for transfer to the memory and display section. If the stored character is not a control code, the control decode circuitry issues a command on the *character write* line to set the character write flip-flop. Its output, fed to the write logic circuitry, indicates that a character awaits transfer to the page memory. At the appropriate instant in the page memory cycle, the data bits are fed in parallel to the memory. At the instant that the character position to be written is displayed on the screen (presently it is a space) the new character is written into the page memory. The time between the "character write" signal and the actual writing of the character varies from zero to 16.67 ms which is the vertical cycle of the display. In the meantime, assembly of a new character can begin in the assembly register.

Baud Rate Estimator

As an aid to determining the operating speed of the incoming signal, a circuit is included which indicates the signal's baud rate. The input data signal is fed to a differentiator (composed of three flip-flops) which generates an output pulse for each mark-to-space and space-to-mark transition. These pulses control a counter, the input of which is driven by a clock signal derived from the 75 WPM clock oscillator through a frequency divider. When the space-to-mark transition occurs at the beginning of a select pulse, the counter is cleared and allowed to count the clock pulses.

As shown in the schematic diagram, Figure 6.7, logic gates are connected to the counter outputs to sense count values in each of five time interval ranges. These gates form the delay calculator. As the counter increments, the gates set flip-flops at specified counts which represent slice points between baud rates. When the next mark-to-space transition occurs, indicating the end of the select pulse, the flip-flops are sampled. The number of flip-flops which have been set determines the time between the space-to-mark and mark-to-space transitions, indicating (within the predetermined ranges) the select pulse duration. For example, when the counter has incremented enough times to indicate that the select pulse length is greater than 11.40 ms, the output of the first gate sets its associated flip-flop. A second gate sets its flip-flop when the counter reaches a count corresponding to a time interval of 15.01 ms or greater. The remaining flip-flops are set in a similar manner if the count becomes high enough.

Four additional gates, one for each operating speed, comprise the baud calculator. These gates are used to determine whether the measured interval corresponds to the select pulse length for a particular operating speed. For example, if the first delay calculator flip-flop is set but the second is not, then the pulse duration is greater than 11.40 ms but less than 15.01 ms. The first of the baud calculator gates detects this condition. Since this time interval range corresponds to the select pulse duration for a 100 WPM signal, the 100 WPM lamp (a light-emitting diode, or LED) is lit. The other three baud calculator gates are inactive and their lights are left in the off state. The same principle applies for each of the other operating speeds. If no time flip-flops are set or all flip-flops are set, this indicates that the select pulse was either too small or too large and the previous state of the LEDs is preserved. It should be noted that since select times are being measured, bias distortion on the signal may cause an incorrect indication.

MEMORY AND DISPLAY SECTION

The memory and display section stores the character codes supplied by the input section, converts each one to a pattern of dots to form the display, and generates a composite video signal to drive the monitor.

The system incorporates three different memories. The first is the page memory, into which the incoming characters are written. Each time a row of characters is to be displayed, forty characters are transferred from the page memory to the line memory, where they are stored temporarily and supplied, one at a time, to the character generator circuitry. A read-only memory in the character generator converts the ASCII codes to the pattern of dots needed for the display.

The remainder of the memory and display section consists of the master clock oscillator, the video timing generator and combiner, and various control circuits, as shown in the block diagram.

Master Clock Oscillator

All functions of the memory and display section are timed and synchronized by the crystal-controlled master oscillator shown in Figure 6. I. It operates at a frequency of 12.2727 MHz.

Page Memory and Control

The page memory stores all 1000 characters which make up a display "page" {25 lines of 40 characters each}. Character codes in parallel format arriving from the input section enter the page memory; they are transferred in groups of 40 to the line memory, where they are used to generate one horizontal row of characters in the display.

The page memory consists of six 1,024-bit shift registers operating in parallel, as shown at the left in Figure 6.4. Since only 1000 characters are stored at any time, the extra 24 locations in each register are unused.

The display, which conforms to U.S. television standards, is recreated or "refreshed" 60 times per second. That is, 60 complete video fields per second are interlaced to produce 30 complete video frames. Both fields of a given frame contain the same information. The contents of the page memory are read out each time a new field is produced, once every 60th of a second.

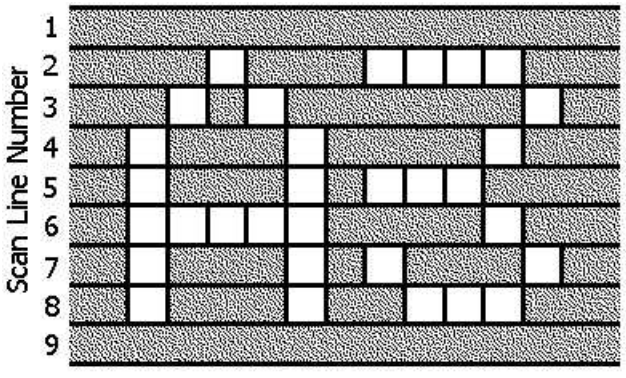
To read out the memory, the shift registers are clocked by pulses derived from the master oscillator. The six bits for each successive character appear in parallel at the register outputs every time a clock pulse occurs. The readout process, however, must be nondestructive – the characters must be retained in the memory for use during subsequent video fields. A feedback path is provided so that characters read out are fed back to the inputs of the registers. At the same time that a character is read out to the line memory it is fed back to the page memory inputs (unless it belongs to a row which is to be deleted or is the one being written by the input section).

Although the memory contains 1,024 locations, only 1,000 are used. The extra 24 locations which are not used must be skipped over during each complete cycle of the memory. Therefore, 24 extra clock pulses are supplied to the memory by the retrace clock generator at the end of each video field during the vertical retrace interval. The memory cycle is then complete and the code for the first character is at the output end of the memory registers, ready to be clocked out again when the next video field starts.

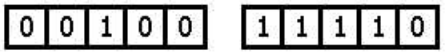
The page memory control circuitry synchronizes the memory cycle with the production of each video field. When a row of characters is to be displayed, it passes 40 clock pulses to the page memory registers, causing 40 characters to be transferred to the line memory and also recycled to the page memory inputs. The memory is not clocked again until the complete row of characters has been produced, a process which requires nine video scan lines. Since there are 25 rows of characters per page, the clocking process is repeated 25 times for each video field.

Line Memory and Control

Nine horizontal scan lines are used to display each row of characters, as Figure 3.3 illustrates. The first line is left dark. The next seven contain the dot patterns which make up the characters, and the remaining one is again left dark. The dark lines separate the rows of characters from each other. The line memory cycles the stored characters while the nine lines are being scanned, feeding the characters in sequence to the character generator ROM at the proper time during each scan.



(a) Dot patterns for characters "A" and "3"



(b) Character generator output codes for scan line 2 of characters "A" and "3"

Figure 3.3 Typical Display Pattern

Six 40-bit shift registers comprise the line memory. As with the page memory, the six registers operate in parallel and are equipped with feedback loops for recycling the stored data. Since the line memory storage capacity is exactly equal to the number of characters to be stored, however, no end-correction circuit is required.

During the first scan line for a new row, the characters to be displayed are transferred from the page memory to the line memory by clocking both memories simultaneously. The character generator produces no output during this scan, so the previous characters stored in the line memory are clocked out without producing dots on the screen.

During each of the next seven scan lines, all 40 characters in the line memory are recycled and also fed to the character generator in succession. During the last line, which is left dark, the memory contents are recycled, but the character generator is again instructed to produce no output.

A control circuit passes clock pulses to the line memory shift registers on the *line clock* bus whenever characters are to be entered or recycled. The line address counter keeps track of the number of shift pulses supplied to the registers. It cycles from zero through 39 as a complete row is transferred from the page memory to the line memory during the first scan line of a row. It also completes a cycle for each of the other eight scan lines needed to produce a row of characters. It therefore records which of the 40 characters in a row is being transferred at a particular instant. Every time this counter recycles, it increments the scan line counter, which keeps track of the scan line number. The control circuit breaks the line memory feedback loop during the first scan line when character data are being entered from the page memory. The scan line counter outputs are fed to the character generator as part of the address code which determines the position of dots on the screen. Each complete cycle of the scan line counter causes the page address counter to increment. Hence, the latter counter increments each time a complete row of characters is displayed, and it therefore records the number of the row being produced.

Character Generator

The character generator is a read-only memory custom precoded to store the dot patterns for 64 different characters. When supplied with the proper input address codes, the memory outputs a digital code corresponding to the dot pattern required for each character.

Since every character is produced by seven scan lines, the dot pattern in each line may be different, as shown in Figure 3.3a. The character ROM must therefore be instructed not only what character to produce, but what scan line of that character is being generated. The character codes come in sequence from the line memory; the scan line number is supplied by the scan line counter in the line memory control circuit.

The characters are five dots wide. The ROM therefore provides five output bits, one for each dot. If a given bit is a "1", a dot is produced on the screen; if the bit is a "0", the space is left dark, as Figure 3.3b illustrates.

The first scan line is left dark by instructing the character generator to display line number zero. All character locations in the character ROM for this scan line are left blank, so no output results regardless of the input data coming from the line memory. During the second scan line, the line memory again cycles and all 40 characters for the row being produced are fed to the character ROM in sequence, along with the scan line number. As the character codes are fed In, the dot codes for the characters appear at the character ROM output.

When the scan line is complete, the scan line counter again increments, the memory is again cycled through all 40 characters, and the character ROM produces the dot pattern for the third scan line. This process is repeated until the eighth scan line is complete. During the ninth scan line, the character ROM is again instructed to produce line zero. No video output results, and the last line is therefore dark.

Cursor Generator

The flashing cursor, which indicates the position of the next character to be entered in the display, is produced by instructing the character ROM to produce the cursor symbol in the position immediately following the last character entered in the bottom row of the display. The cursor logic senses the state of the input character counter and drives the chip enable input of the character ROM at the desired instant during the line memory cycle as the characters in the 25th row of the display are being supplied to the character ROM. Disabling the ROM causes its outputs to go high, resulting in a white line. The cursor is made to flash by an oscillator which alternately enables and disables the cursor logic.

Data Entry Control

Characters supplied from the input section must be transferred to the page memory at the correct instant in its cycle if they are to appear at the proper position on the screen. A character which has been received, assembled and converted in the input section, is stored there momentarily until the page memory is ready to accept it. The write logic synchronizes the transfer of the character to the page memory.

Character codes are transferred to the page memory just previous to the production of the bottom (25th) row of characters on the screen. The transfer occurs during the first (blank) scan line of that row, when the page memory contents for the 25th row are being entered in the line memory.

An input character counter keeps track of the number of characters which have been entered from the input section. As with the line address counter, it cycles from 0 through 39. It is reset to zero at the beginning of each new row. At that point in the operating cycle when (1) the page address counter reads 24, indicating that the last (25th) row of characters is being produced, (2) the scan line counter reads 0, indicating that the first scan line of the row is being generated, (3) the line address counter contains the same number as the input character counter, and (4) the character write flip-flop indicates that a converted character is waiting in the input section, the transfer occurs. New characters therefore always appear in the bottom line of the display.

The new character is read into the page memory by breaking the feedback path of the memory shift register when the input character counter and the line address counter coincide. The previously stored character (a space) is therefore not fed back to the page memory input on the next shift pulse. The new character is entered in its place. The feedback path is then reestablished before the next shift pulse occurs.

To illustrate this process, let us assume that the screen is filled except for the last line, and that nine characters have al ready been written in that line. A new character is assembled in the input section and the character write flip-flop is set. The input character counter contains the number line, indicating that nine characters have already been entered in the row and that the new one will be the tenth. When the character has been entered, the counter is advanced to 10.

As the page memory starts through its cycle, the line address and page address counters increment. When the page address counter reaches 24, indicating that the last line is being read out, and the line address counter reads nine, showing that the first nine characters in the last row have been read out, the feedback path is broken, the next stored character is deleted, and the new one is entered in its place. The feedback path is then reconnected, and the memory continues through its cycle. The next new character will be entered in the same manner on a later memory cycle.

Since the page memory completes a cycle every 16.7 ms, the delay while the converted character in the input section awaits transfer to the page memory is short compared to the time it takes to assemble the next incoming character (about 100 ms at 100 WPM).

Line Feed Control

A line feed command can originate from any of three sources: (1) the control code detector in the input section whenever a line feed code is received or when a space is received after the 34th character in a line, (2) the page address and line address counters when they recycle, indicating that the last line of the display has been filled, and (3) the manual line feed pushbutton. The line feed logic circuit detects any of these conditions.

When a line feed request signal has been produced by one of these sources and when the various counters indicate that the last scan line of the character display is complete, the page memory feedback path is broken and the memory is clocked an extra 40 times. The 40 characters which would otherwise have constituted the first row of the next display field are clocked out of the memory. Since the feedback path is broken, these characters are lost. Space characters are supplied to the register inputs during this clocking operation so that the last line of the next display field will be blank. All other characters are moved up one line in the process.

Whenever a line feed occurs, the input character counter is reset to zero. Consequently the next new character is written at the leftmost position of the bottom line. In this way, a carriage return is automatically produced with each line feed, regardless of how the line feed command originated.

Output Shift Register

As the line memory cycles, the five dot code bits for each character appear in parallel at the character ROM output. To produce dots at the proper time (and hence the proper position on the scan lines), the dot code bits must be fed serially to the video output circuits. A five-bit shift register performs the parallel-to-serial conversion.

Upon a command from the line memory control, the character ROM output bits are loaded into the shift register. They are then clocked out of the register into the video combiner by pulses from the master clock. After all five bits have been transferred and before the register is reloaded with the dot code for the next character, two extra clock pulses are allowed to pass. These extra pulses result in a blank space two dots wide between characters.

Video Circuitry

The dot code which comes from the character generator via the output shift register must be mixed with video synchronization and blanking signals and fed to the external monitor. The video circuits perform these functions.

A special IC contains all the circuitry needed to produce the video synchronization and blanking pulses. Its input is driven at 2.0475 MHz by a scaler which divides the master oscillator frequency by a factor of six.

The sync generator outputs are shown in Figure 3.4. One horizontal sync pulse and one horizontal blanking pulse are produced for each of the 525 lines in a video frame. One vertical blanking pulse is produced for each of the 60 fields scanned every second. Since standard television format uses interlace scanning, the blanking signals for alternate fields are offset from each other by one-half of a horizontal scan time. The sync generator outputs are fed to the video combiner as well as to the horizontal and vertical position controls, where they are used to position the display in the center of the screen.

The video combiner mixes the video, blanking, and synchronization signals and drives the external video monitor. The combiner is composed of three switched constant current sources, each of which is driven by one of the three input signals. The video monitor input impedance serves as a common load for all three current sources, so the output to the monitor is the sum of the three Input signals. Figure 1.4 shows the composite video waveform.

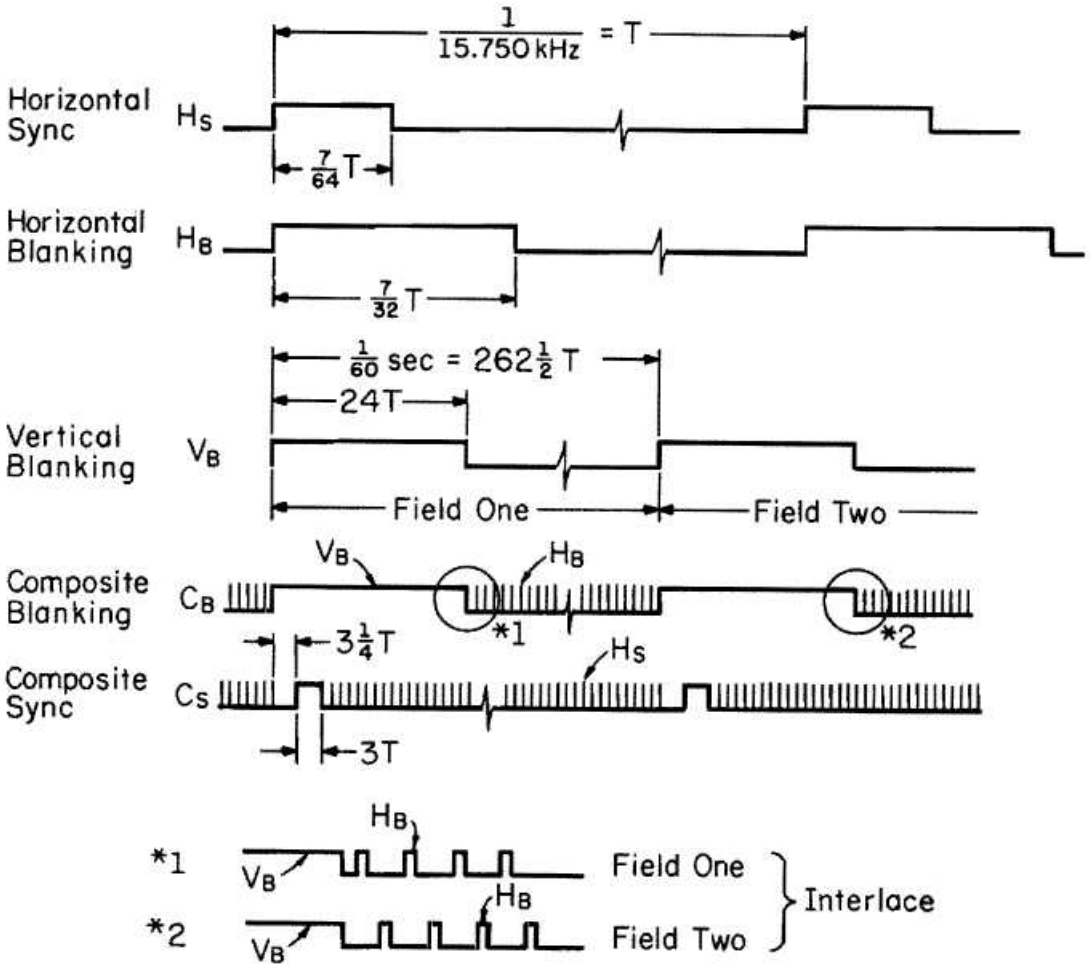


Figure 3.4 Video Timing Signals

4. Maintenance

Your RVD-1005 has been carefully engineered and is constructed from high-quality components to ensure years of trouble-free service when installed and operated properly. The unit requires no routine maintenance, and in current production models there are no internal adjustments. On models with serial numbers less than 241, a control is included to adjust the +5 volt output voltage of the regulated power supply. The setting of this control will not need to be changed under normal circumstances but should be checked in case the unit malfunctions. The procedure is explained below.

In Case of Difficulty ...

Because the logic circuitry of the RVD-1005 is quite complex, extensive troubleshooting should be done only by an experienced technician who is familiar with high-speed digital logic circuitry and who has the proper test equipment, including a wideband, triggered-sweep high-performance oscilloscope, at his disposal. Please note that the warranty is void if repairs are attempted by an unauthorized person.

If the unit fails to operate properly, it is usually most satisfactory to return it to HAL Communications Corp. for repair after making the basic tests described below. If you plan to send your unit in for factory service, please notify the company by telephone or letter and wait to ship it until you receive a return authorization card.

Basic Troubleshooting

Before opening the cabinet to make internal measurements, make the following checks:

1. Be sure that the line cord is connected to an AC power source of the correct voltage and frequency. Units designed for 220 V AC operation are identified by a tag on the rear panel or the line cord.

2. Check the fuse in the holder on the rear panel.

3. Reread the operating instructions in Section 2 to make certain that you are using the unit correctly.

4. Reinspect the connections to the input signal source (RTTY loop circuit or demodulator) and to the video monitor.

5. Check the input signal from the loop or demodulator with an oscilloscope or by feeding it to another printer system and observing whether that system performs properly. Be sure to determine whether the voltage or current levels fall within the range specified in Section 1.

6. Test the monitor, if possible, by disconnecting the feed cable from the visual display unit and driving the monitor with a test signal.

If these checks do not reveal the source of the problem, a few internal tests may be made if the appropriate test equipment is available:

1. Remove the top cover. CAUTION: High voltages are exposed when the cover is removed. Make the following measurements with great care. To prevent possible injury or damage to the unit, be certain that the test probe does not short between adjacent connections or conductors.

2. Switch the unit on. Ground the negative lead of an accurate (±3 %) voltmeter to the cabinet and measure the voltages present at each of the points listed in Table 4.1. The test points are shown in Figures 7. I, 7.2 and 7.3.

Table 4.1 Voltage Measurements

Parameter	Measurement Point	Acceptable Range
+5 volts	Power Supply Board Logic Circuit Board	+4.9 to +5.2 volts
–5 volts	Logic Circuit Board	–4.9 to –5.7 volts
–12 volts	Power Supply Board Logic Circuit Board	–12.0 to –12.2 volts

Early models of the RVD-1005 used a power supply circuit board with a potentiometer for adjustment of the +5 volt power supply. This potentiometer (the only potentiometer on the power supply board) should be set for a +5.0 volt output as measured on the logic circuit board. The circuit of this model of the power supply is detailed in Figure 6.8, detail A.

Units with serial numbers higher than 241 use power supplies with fixed voltage outputs. If voltages are measured that are not within the indicated acceptable range, first check the accuracy of the voltmeter. If the problem persists, the probable cause is a short, defective component, or overload. Check for overload by turning the RVD-1005 off, disconnecting the power cable to the logic board, and remeasuring the voltages at the power supply with the logic board disconnected. All voltages may measure as much as 10 % higher with the logic board disconnected. Note that the -5 volts is derived on the logic board from the –12 volt supply and will therefore not be found on the power supply board. The three versions of power supplies that have been supplied with the RVD-1005 are diagramed in Figures 6.8 and 6.9. Models with serial numbers less than 241 use the supply of Figure 6.8, detail A; serial numbers between 241 and 345 use the supply of Figure 6.8 and 7.2; serial numbers higher than 345 use the circuit board shown in Figure 6.8 and 7.3.

3. If the voltages are correct, the operation of the internal oscillators may be checked by observing their output waveforms with an oscilloscope having a vertical bandwidth of 10 MHz or greater. Check for the presence of output from the input clock oscillators at the point labeled INPUT CLOCK in Figure 7.1. Check each of the four oscillators in turn (one for each operating speed) by depressing the speed selector switches in succession and looking for the presence of a waveform on the oscilloscope. The frequencies should be in the range from 5.9 to 9.7 MHz. The exact frequencies are listed in Section 3. Table 3.2.

Check the master clock oscillator by connecting the oscilloscope probe to the point labeled MASTER CLOCK in Figure 7. I. A 6.1425 MHz signal should be present. This signal is derived from a 12.2727 MHz crystal oscillator through a divide-by-two circuit.

If any of these signals is not present, check the oscillator circuitry. A schematic of the input timing oscillators is shown in Section 6, Figure 6.6, and the master clock is shown at the right in Figure 6.1.

Problems not isolated by these simple tests should normally be referred to the factory. Further information on the operating principles of the circuitry is given in Section 3. A complete set of schematic diagrams is included in Sect ion 6.

5. Using a Television Set as a Monitor

Most standard American television sets can be easily modified to serve as video monitors. The change does not affect normal operation of the set except that the cable should be removed from the TV set for normal viewing.

CAUTION: Do not attempt to use as a monitor any television receiver in which one side of the AC line is connected to the chassis or circuit ground unless you supply AC power to the set from a reliable isolation transformer.

The modification is simply a matter of capacitively coupling the external video signal to the input of the first video amplifier stage. Figure 5.1 shows a typical transistorized video circuit. Although the component values and the biasing method may be slightly different in your set, the circuit will be essentially as shown. The video signal is injected at point A.

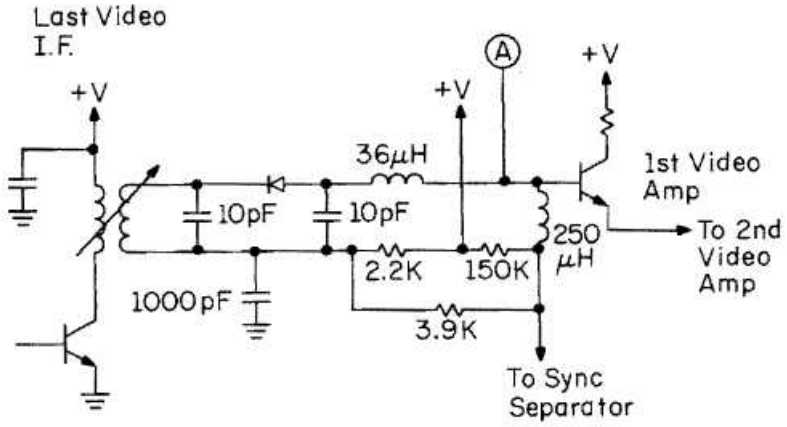


Figure 5.1 Typical Transistor Video Detector

The modified circuit is shown in Figure 5.2. Connect the negative end of a 100 µF, 16 volt electrolytic capacitor to the base of the first video amplifier transistor. Mount a BNC connector on the cabinet as close as possible to the transistor. Using a short length of hookup wire, connect the center pin of the BNC connector to the positive end of the capacitor. If the distance is short, the capacitor leads themselves may take the place of the hookup wire. On the other hand, if the distance is greater than six inches, substitute a length of coaxial cable. Miniature coax, such as RG-174/U, may be used even though its characteristic impedance is 50 ohms.

Figure 5.3 shows a typical video circuit using tubes. The external video signal is injected at point A. Connect the negative end of a 10 µF, 100 volt electrolytic capacitor to the detector side of the existing coupling capacitor, as shown in Figure 5.4. Note that a 75 ohm resistor is wired across the input connector to provide the proper load impedance for the RVD-1005 output.

Some tube-type sets may require a video level of 3 volts peak-to-peak to provide good contrast. In that case a two-stage video amplifier. such as that shown in Figure 5.5, may be inserted in the line from visual display system to the television set.

In some sets the video at the coupling point may have reverse polarity, with positive-going synchronization pulses and negative video information. This situation will often be found in transistorized sets which use a negative power supply and PNP transistors. The unity-gain phase inverter shown in Figure 5.6 may be inserted in the line from the RVD-1005 to reverse the video signal polarity.

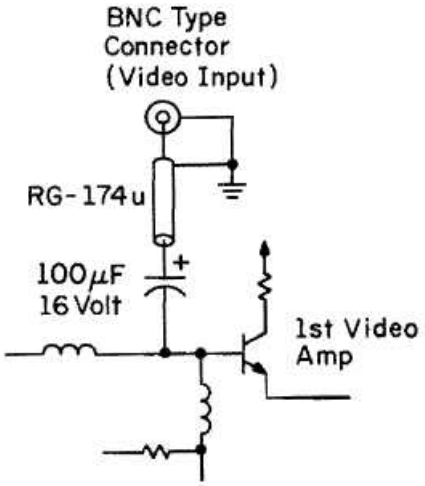


Figure 5.2 Modified Transistor Video Detector

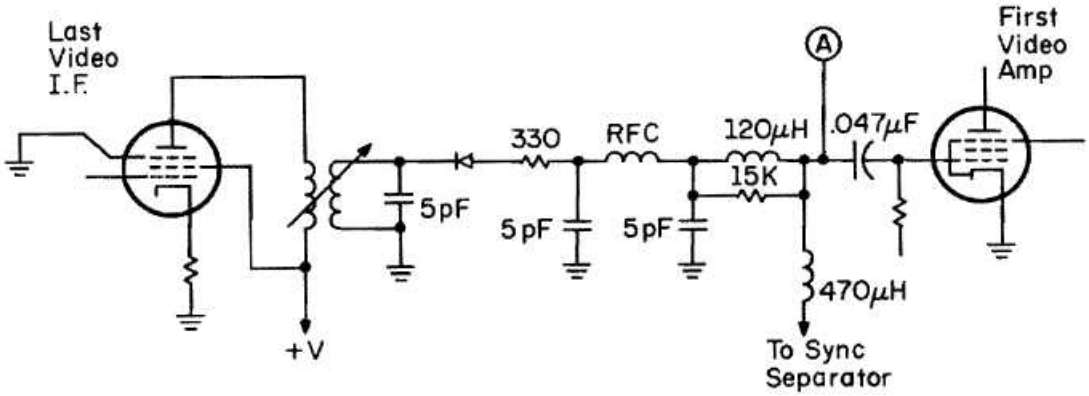


Figure 5.3 Typical Tube-type Video Detector

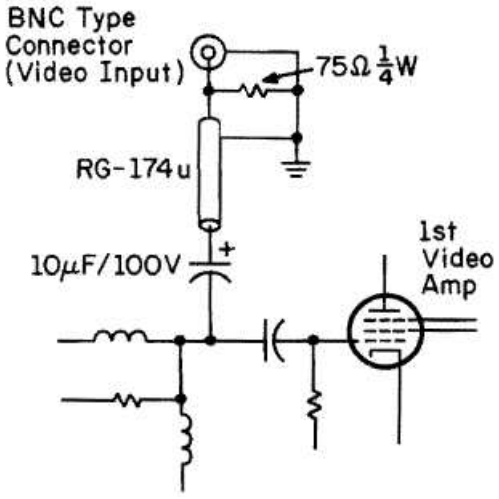


Figure 5.4 Modified Tube-type Video Detector

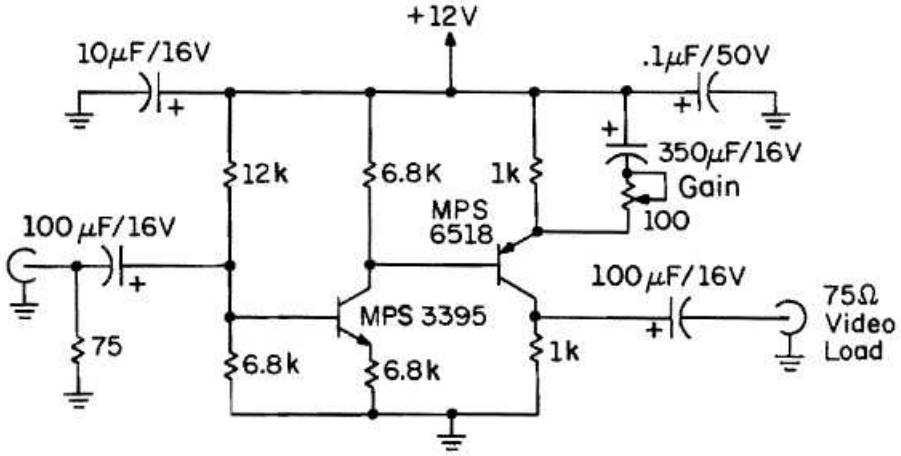


Figure 5.5 Video Amplifier

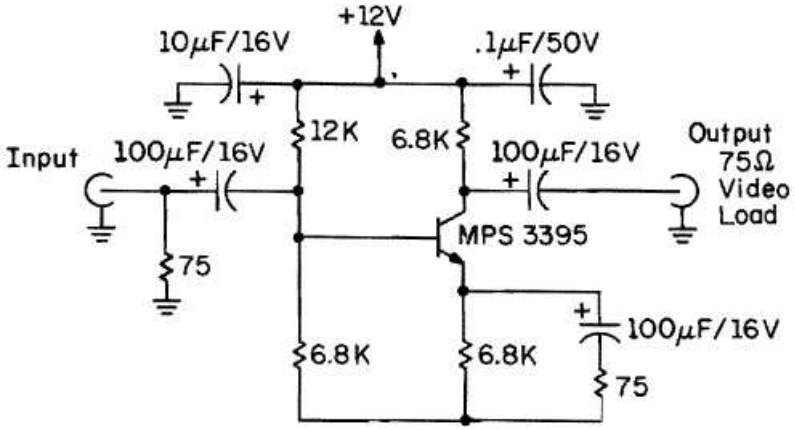


Figure 5.6 Video Inverter

6. Schematic Diagrams

In this section you will find the schematic diagrams for the RVD-1005, as listed below. The drawing conventions are depicted in Figure 6.10.

Figure 6.1: Video, Line Feed, and Retrace Control

Figure 6.2: Page Position Control

Figure 6.3: Line Position Control

Figure 6.4: Character Memory

Figure 6.5: Input Control Decode

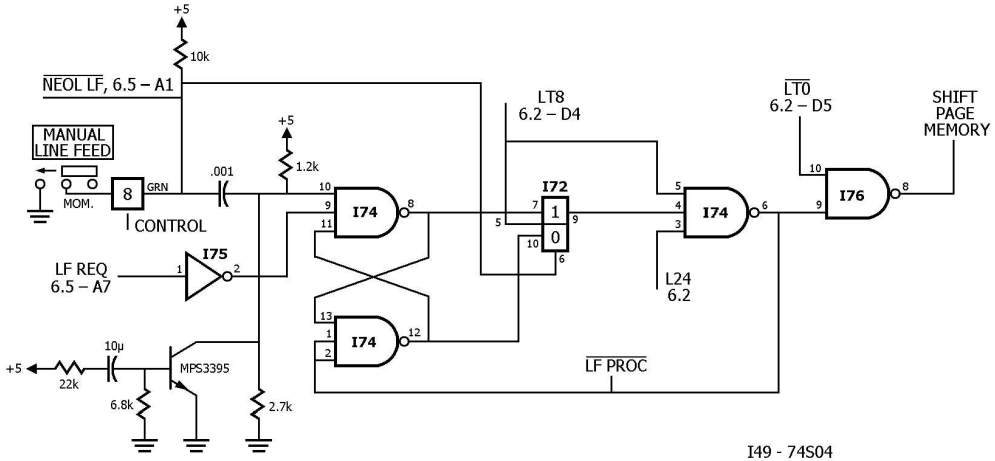
Figure 6.6: Input Timing Chain

Figure 6.7: Baud Rate Estimator

Figure 6.8: Power Supply (serial numbers less than 345)

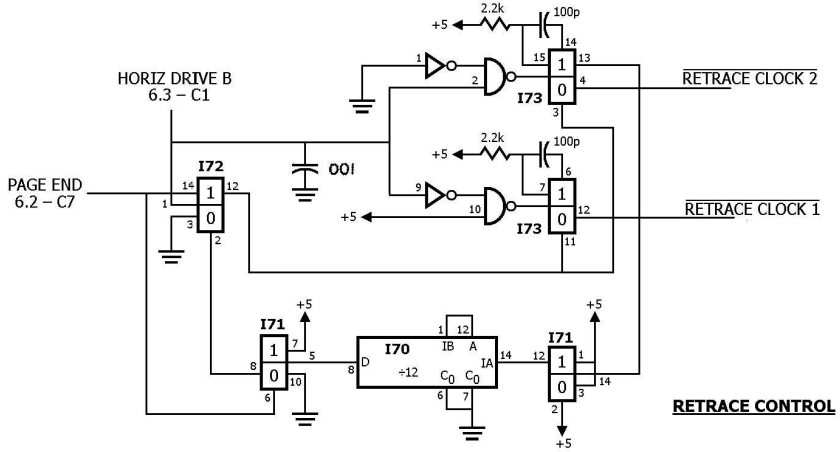
Figure 6.9: Power Supply (serial numbers 346 and higher)

Figure 6.10: Drawing Conventions



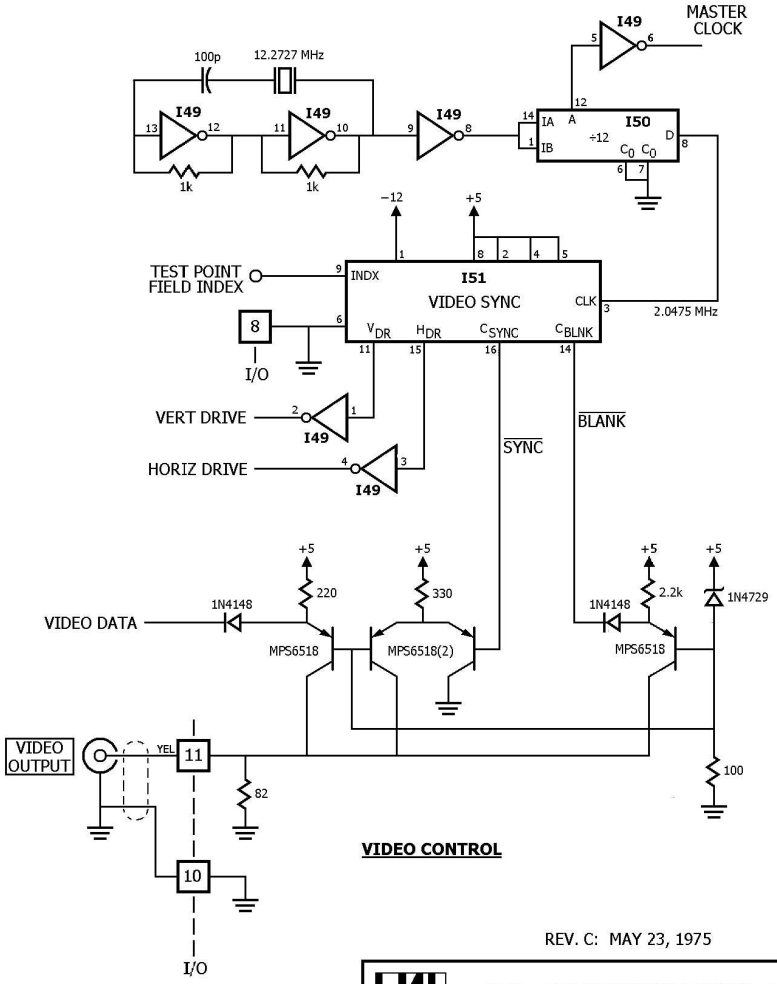
LINE FEED CONTROL

I49 - 74S04
I50, I70 - 7492
I51 - MM5320
I71, I72 - 7473
I74 - 7410
I75 - 7404
I76 - 7400



RETRACE CONTROL

NOTE: 1. ACCEPTABLE SUBSTITUTES ARE
- MPS3394 FOR MPS3395
- MPS3702 OR MPS3703 FOR MPS6518
2. ALL RESISTORS ARE 1/4 W ±5 %



VIDEO CONTROL

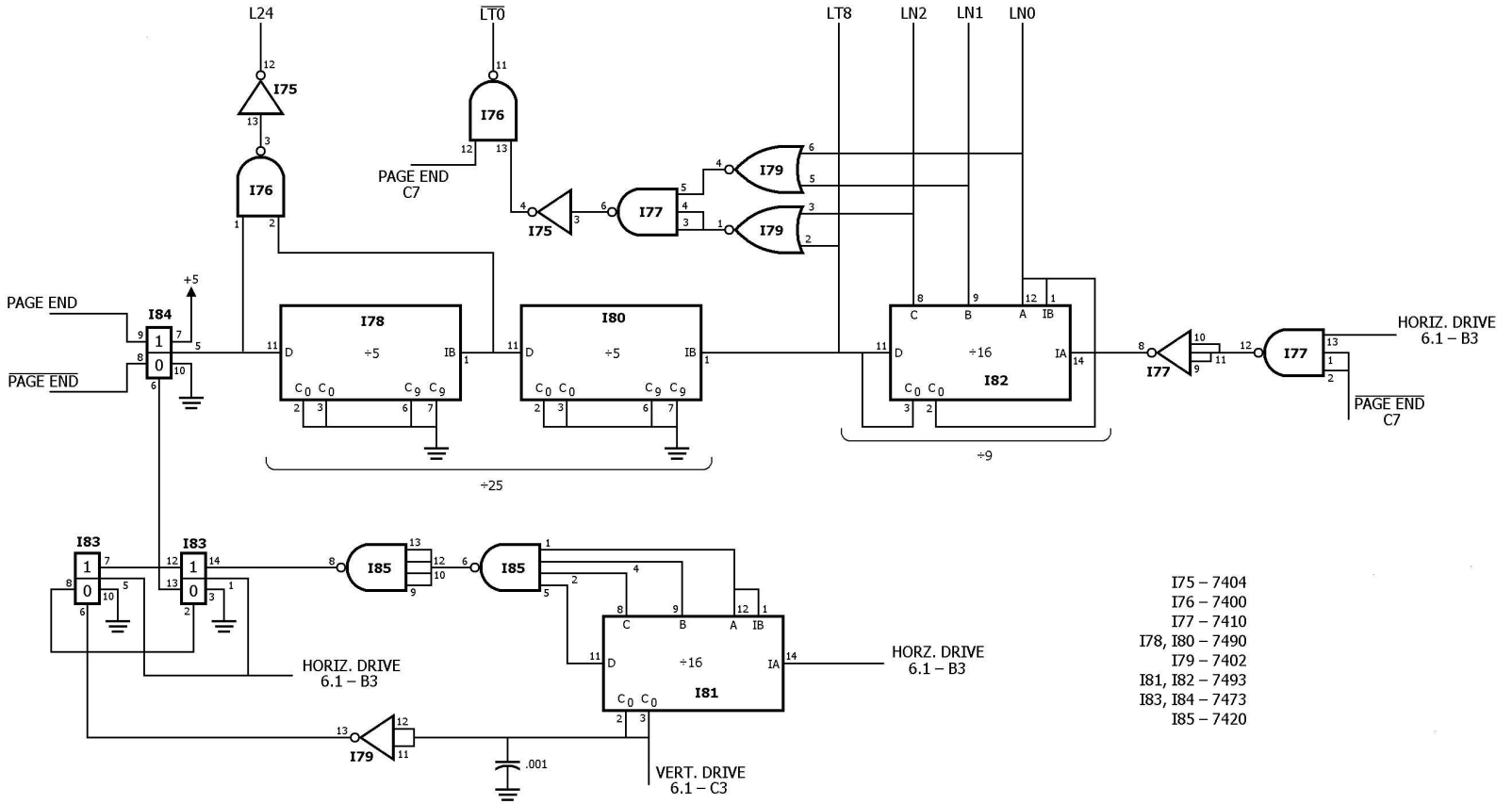
Figure 6.1

REV. C: MAY 23, 1975

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801

RVD – 1005
VIDEO, LINE FEED AND RETRACE CONTROL

DATE JAN. 14, 1975 | No. A1016C



I75 – 7404
I76 – 7400
I77 – 7410
I78, I80 – 7490
I79 – 7402
I81, I82 – 7493
I83, I84 – 7473
I85 – 7420

Figure 6.2

REV. C: MAY 23, 1975

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801

RVD – 1005
PAGE POSITION CONROL

DATE JAN. 15, 1975 | No. A1017C

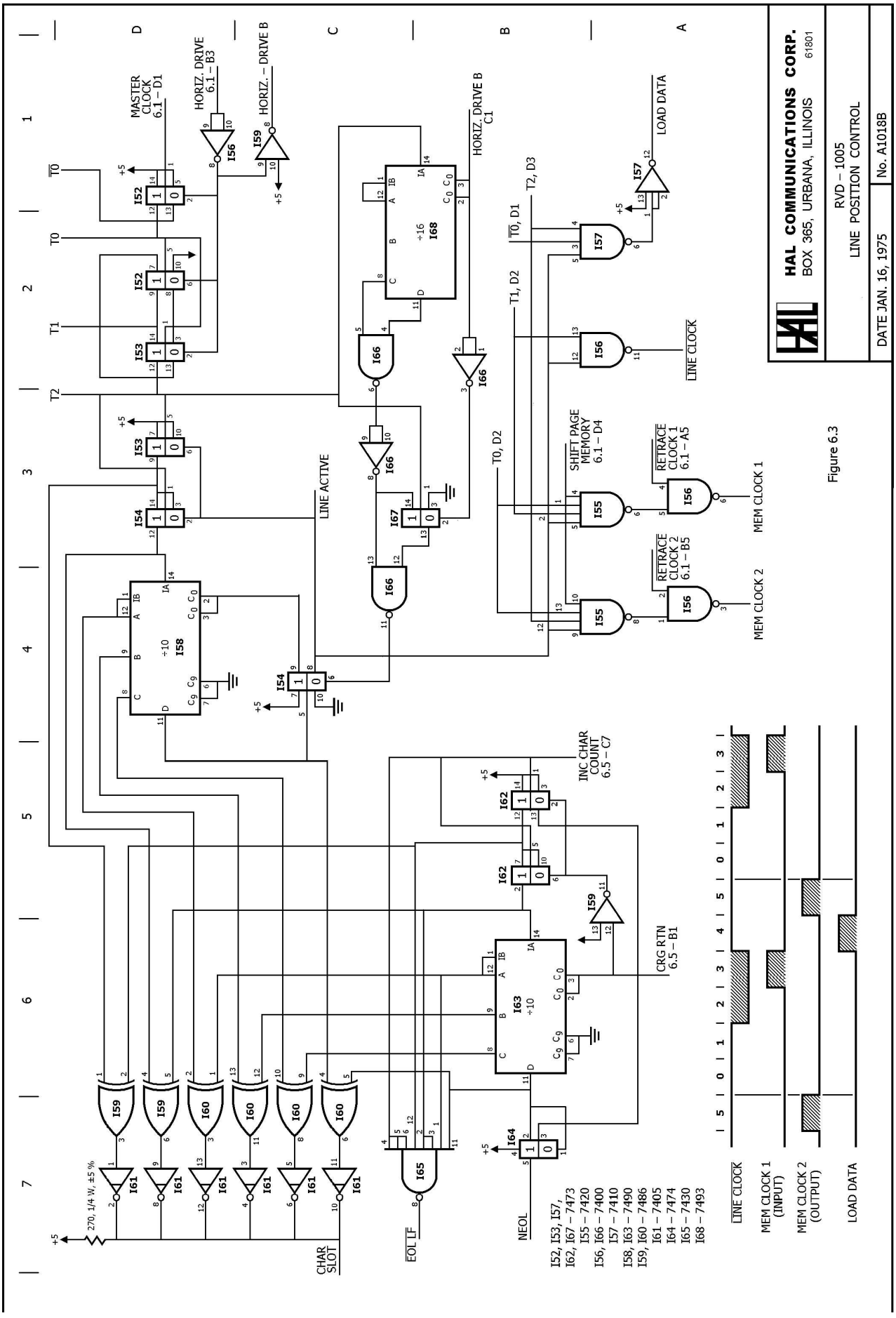
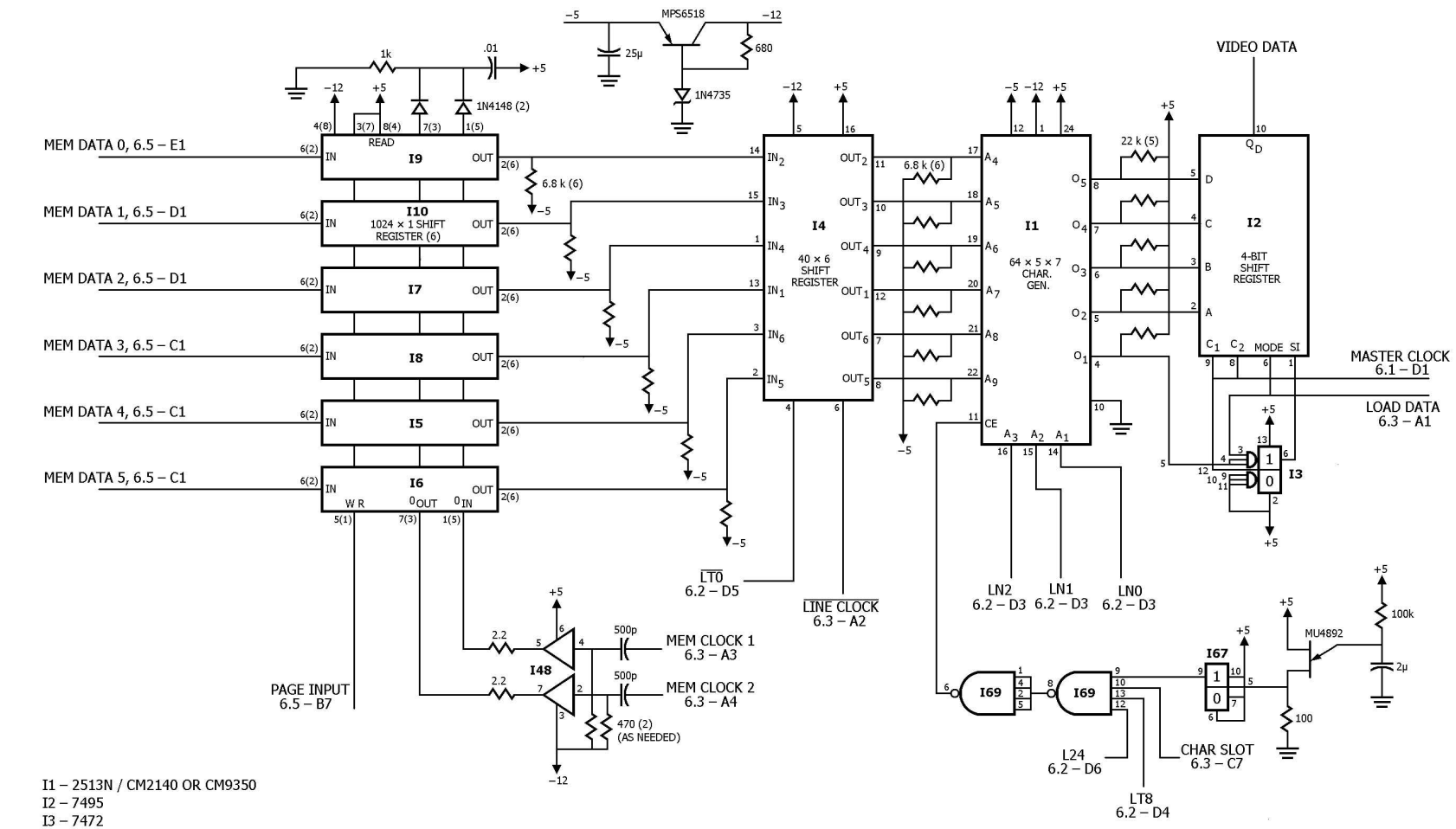

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801
RVD – 1005
LINE POSITION CONTROL
DATE JAN. 16, 1975
No. A1018B
MASTER CLOCK 6.1 – D1
HORIZ. DRIVE 6.1 – B3
HORIZ. – DRIVE B
HORIZ. DRIVE B C1
LOAD DATA
LINE ACTIVE
LINE CLOCK
SHIFT PAGE MEMORY 6.1 – D4
RETRACE CLOCK 1 6.1 – A5
RETRACE CLOCK 2 6.1 – B5
MEM CLOCK 1
MEM CLOCK 2
INC CHAR COUNT 6.5 – C7
CRG RTN 6.5 – B1
CHAR SLOT
EOL LF
NEOL
270, 1/4 W, ±5 %
I52, I53, I57,
I62, I67 – 7473
I55 – 7420
I56, I66 – 7400
I57 – 7410
I58, I63 – 7490
I59, I60 – 7486
I61 – 7405
I64 – 7474
I65 – 7430
I68 – 7493
LINE CLOCK
MEM CLOCK 1 (INPUT)
MEM CLOCK 2 (OUTPUT)
LOAD DATA

Figure 6.3



I1 – 2513N / CM2140 OR CM9350
I2 – 7495
I3 – 7472
I4 – 2519B
I5 - I10 – MM5013
I48 – MH0026CN
I67 – 7476
I69 – 7420

NOTE: 1. ACCEPTABLE SUBSTITUTES ARE
- MPS3702 OR MPS3703 FOR MPS6518
- 2525V FOR MM5013 (PIN NUMBERS IN PARENTHESES ARE FOR MM5013)
2. ALL RESISTORS ARE 1/4 W, ±5 %

Figure 6.4

REV. C: MAY 23, 1975

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801

RVD – 1005
CHARACTER MEMORY

DATE JAN. 16, 1975 | No. A1019C

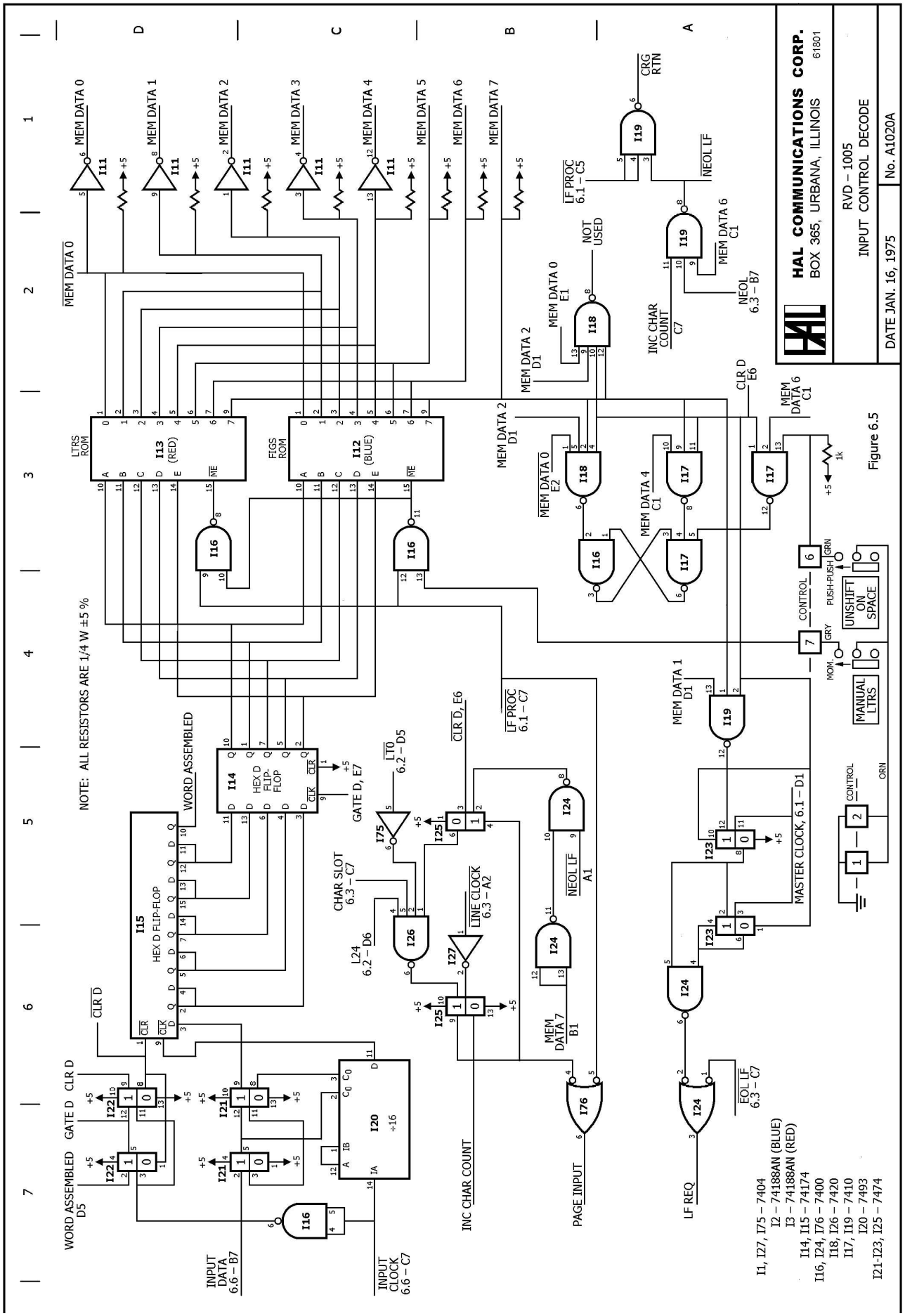

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801
RVD – 1005
INPUT CONTROL DECODE
DATE JAN. 16, 1975
No. A1020A
NOTE: ALL RESISTORS ARE 1/4 W ±5 %
MEM DATA 0
MEM DATA 1
MEM DATA 2
MEM DATA 3
MEM DATA 4
MEM DATA 5
MEM DATA 6
MEM DATA 7
LTRS ROM
FIGS ROM
I13 (RED)
I12 (BLUE)
I15 HEX D FLIP-FLOP
I14 HEX D FLIP-FLOP
I20 ÷16
WORD ASSEMBLED
GATE D, E7
CLR D
CLR D, E6
CHAR SLOT 6.3 – C7
LINE CLOCK 6.3 – A2
L24 6.2 – D6
LT0 6.2 – D5
LF PROC 6.1 – C7
NEOL LF A1
MEM DATA 7 B1
INC CHAR COUNT
PAGE INPUT
INPUT DATA 6.6 – B7
INPUT CLOCK 6.6 – C7
WORD ASSEMBLED D5
LF REQ
EOL LF 6.3 – C7
MASTER CLOCK, 6.1 – D1
LF PROC 6.1 – C5
NOT USED
CRG RTN
NEOL LF
MEM DATA 6 C1
NEOL 6.3 – B7
INC CHAR COUNT C7
MEM DATA 0 E1
MEM DATA 2 D1
MEM DATA 0 E2
MEM DATA 4 C1
CLR D E6
MEM DATA 6 C1
MEM DATA 1 D1
CONTROL
PUSH-PUSH
GRN
GRY
MOM.
UNSHIFT ON SPACE
MANUAL LTRS
ORN
I1, I27, I75 – 7404
I2 – 74188AN (BLUE)
I3 – 74188AN (RED)
I14, I15 – 74174
I16, I24, I76 – 7400
I18, I26 – 7420
I17, I19 – 7410
I20 – 7493
I21-I23, I25 – 7474

Figure 6.5

I26 – 7420
I27 – 7404
I28 – 7400
I29 - I32 – 7493
I47 – FCD810

NOTE:
1. RI = 120 FOR EIA INPUT
   RI = 0 FOR TTL INPUT
2. SWITCHES THIS SHEET ARE INTERLOCKING WITH POWER SWITCH
3. ALL RESISTORS ARE 1/4 W, ±5 %

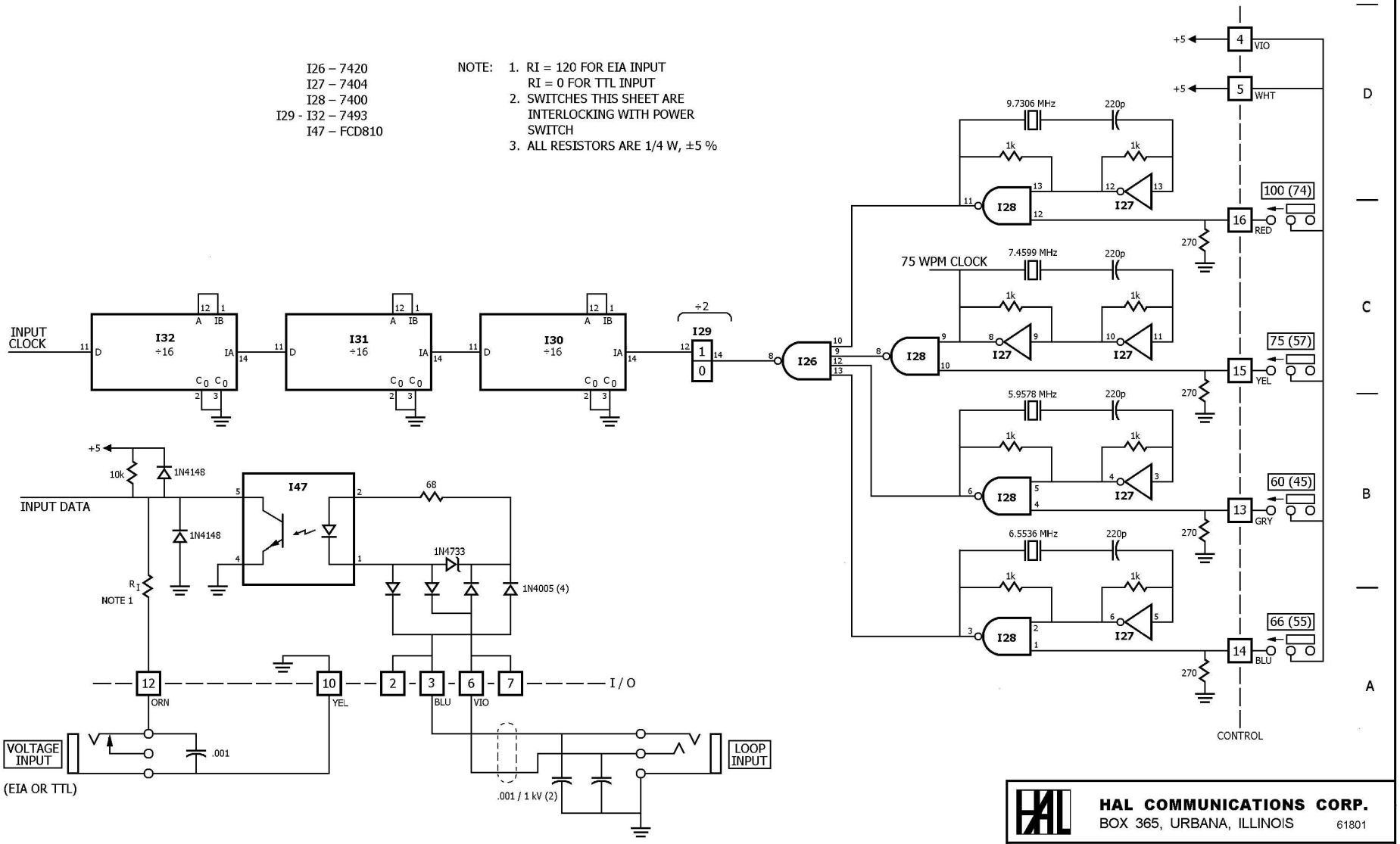


Figure 6.6

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801

RVD – 1005
INPUT TIMING CHAIN

DATE JAN. 19, 1975 | No. A1021A

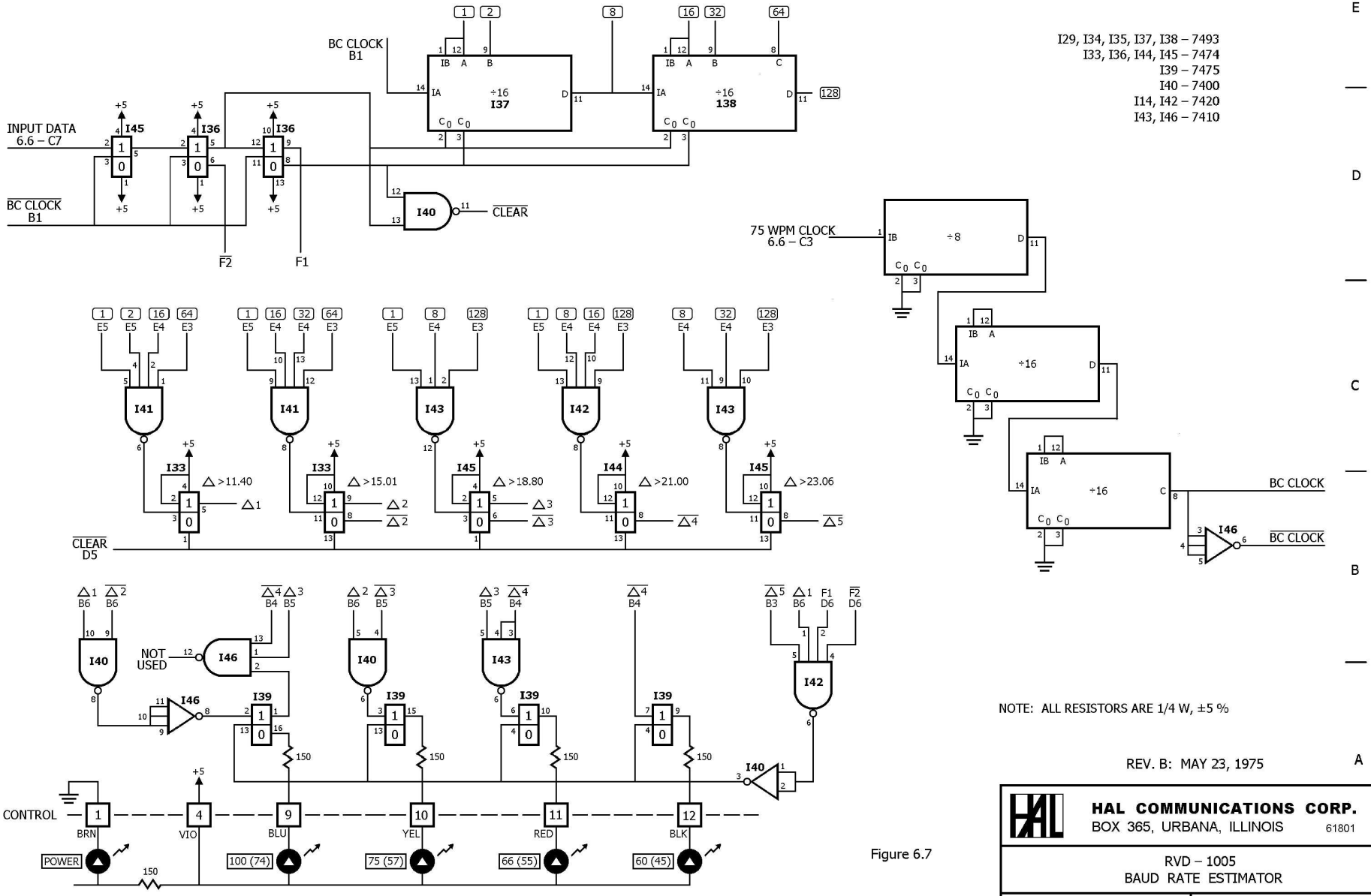
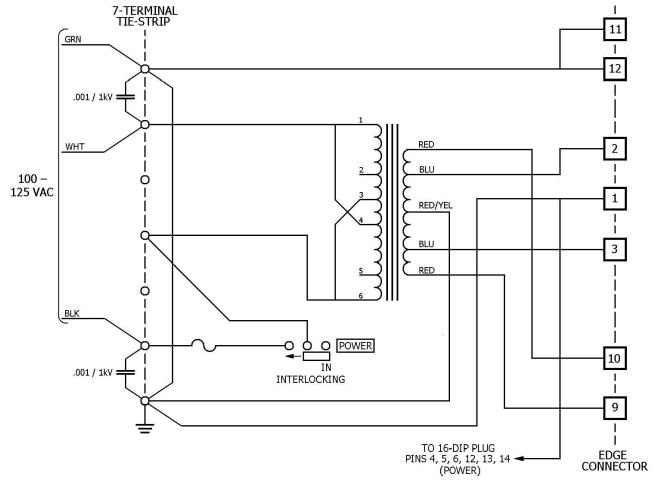
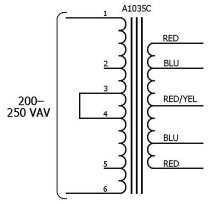

7
6
5
4
3
2
1
E
D
C
B
A
I29, I34, I35, I37, I38 – 7493
I33, I36, I44, I45 – 7474
I39 – 7475
I40 – 7400
I14, I42 – 7420
I43, I46 – 7410
BC CLOCK B1
INPUT DATA 6.6 – C7
BC CLOCK B1
I37
I38
I40
CLEAR
F2
F1
75 WPM CLOCK 6.6 – C3
BC CLOCK
BC CLOCK
I41
I43
I42
I33
I44
I45
I46
>11.40
>15.01
>18.80
>21.00
>23.06
CLEAR D5
NOT USED
I39
150
CONTROL
BRN
VIO
BLU
YEL
RED
BLK
POWER
100 (74)
75 (57)
66 (55)
60 (45)
NOTE: ALL RESISTORS ARE 1/4 W, ±5 %
REV. B: MAY 23, 1975
HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801
RVD – 1005
BAUD RATE ESTIMATOR
DATE JAN. 21, 1975
No. A1022B

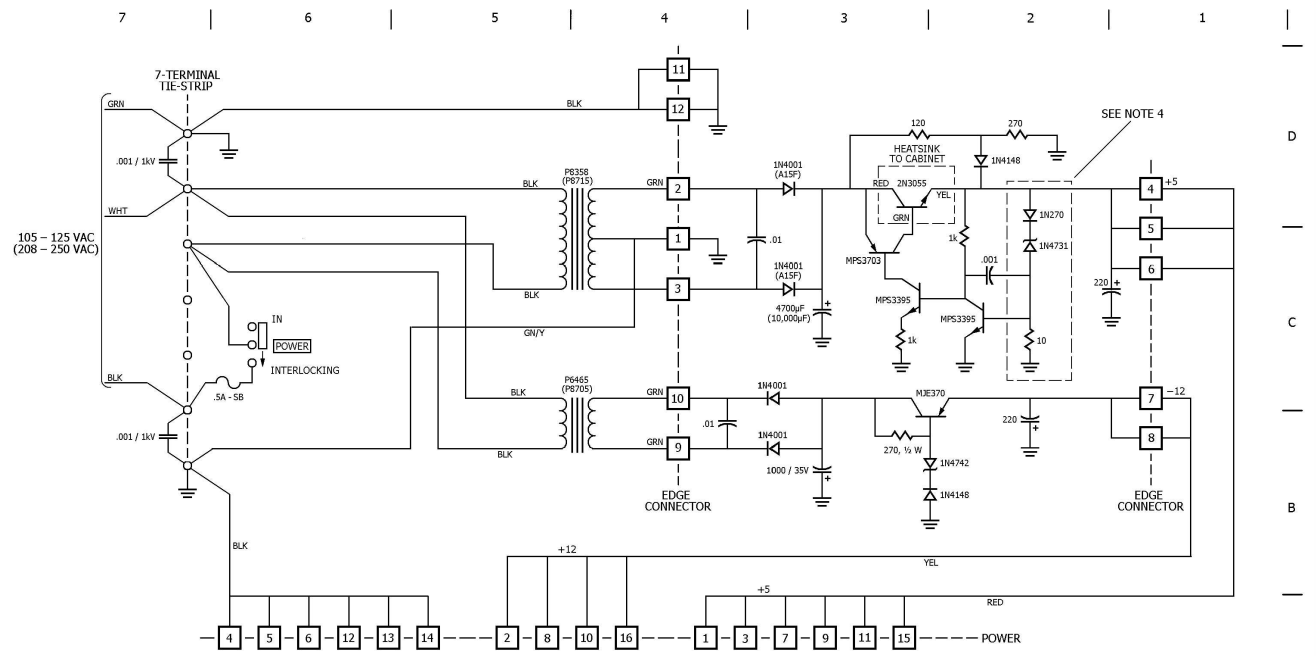
Figure 6.7



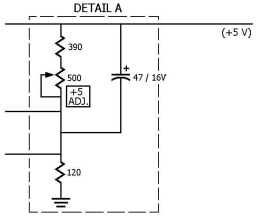
200 – 250 VAC TRANSFORMER CONNECTION



Alternate Connections with A1035 Power Transformer



NOTE:
1. ACCEPTABLE SUBSTITUTES ARE MPS3702, MPS6518 FOR MPS3703 MPS3394, MPS6514 FOR MPS3395
2. ALL RESISTORS ARE 1/4 W ±5 % UNLESS OTHERWISE NOTED
3. SPECIFICATIONS IN PARENTHESES ARE FOR 220 VAC OPERATION
4. UNITS WITH SERIAL NO.'s <241 HAVE ADJUSTMENT FOR THE +5 V REGULATOR AS PER DETAIL A



REV. A: MAY 23, 1975

HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801

RVD – 1005
POWER SUPPLY (SERIAL NO.'s < 346)

DATE FEB. 3, 1975 | No. A1088

Figure 6.8

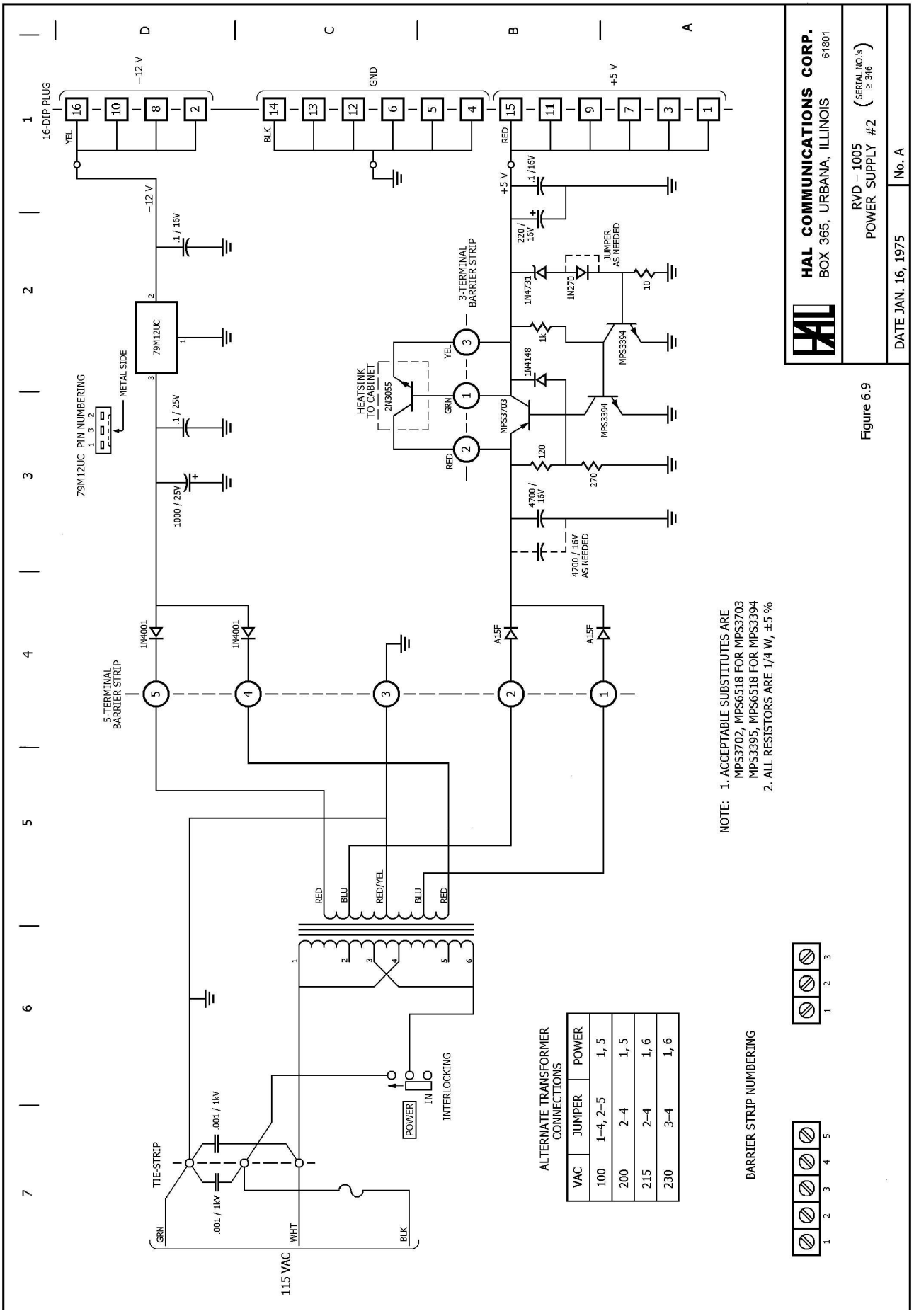

16-DIP PLUG
−12 V
GND
+5 V
79M12UC PIN NUMBERING
METAL SIDE
79M12UC
HEATSINK TO CABINET
2N3055
3-TERMINAL BARRIER STRIP
5-TERMINAL BARRIER STRIP
1N4001
A15F
1N4148
1N4731
1N270
MPS3703
MPS3394
JUMPER AS NEEDED
4700 / 16V AS NEEDED
TIE-STRIP
115 VAC
POWER
INTERLOCKING
NOTE: 1. ACCEPTABLE SUBSTITUTES ARE MPS3702, MPS6518 FOR MPS3703 MPS3395, MPS6518 FOR MPS3394
2. ALL RESISTORS ARE 1/4 W, ±5 %
ALTERNATE TRANSFORMER CONNECTIONS
VAC | JUMPER | POWER
100 | 1–4, 2–5 | 1, 5
200 | 2–4 | 1, 5
215 | 2–4 | 1, 6
230 | 3–4 | 1, 6
BARRIER STRIP NUMBERING
HAL COMMUNICATIONS CORP.
BOX 365, URBANA, ILLINOIS 61801
RVD – 1005 POWER SUPPLY #2 (SERIAL NO.'s ≥ 346)
DATE JAN. 16, 1975
No. A

Figure 6.9

7. Printed Circuit Card layouts

The following photographs show the position of components on the printed circuit cards as well as typical cabinet interior details. Some late model changes may not be shown in these photographs.

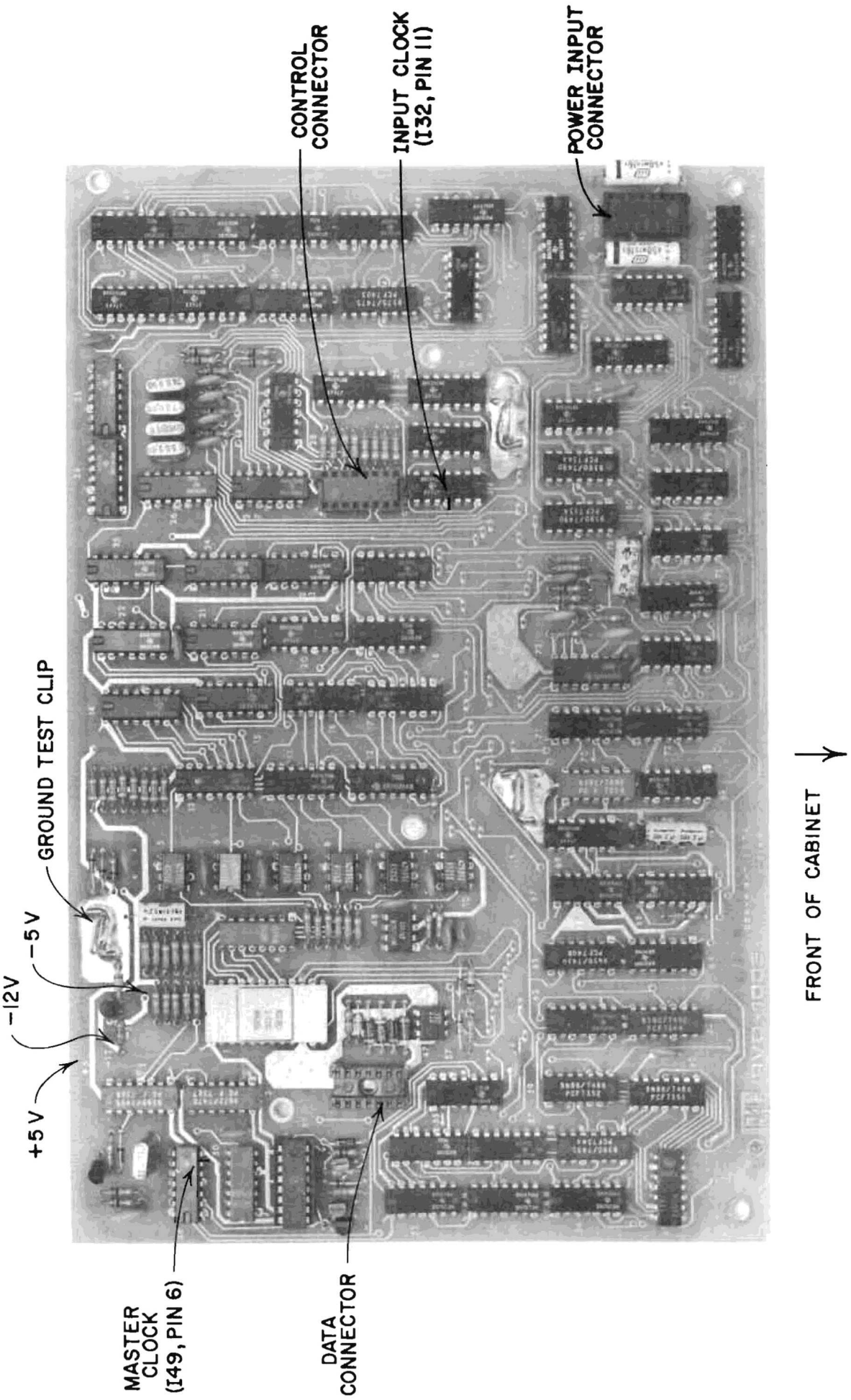


Figure 7.1 Logic Circuit Board Photograph

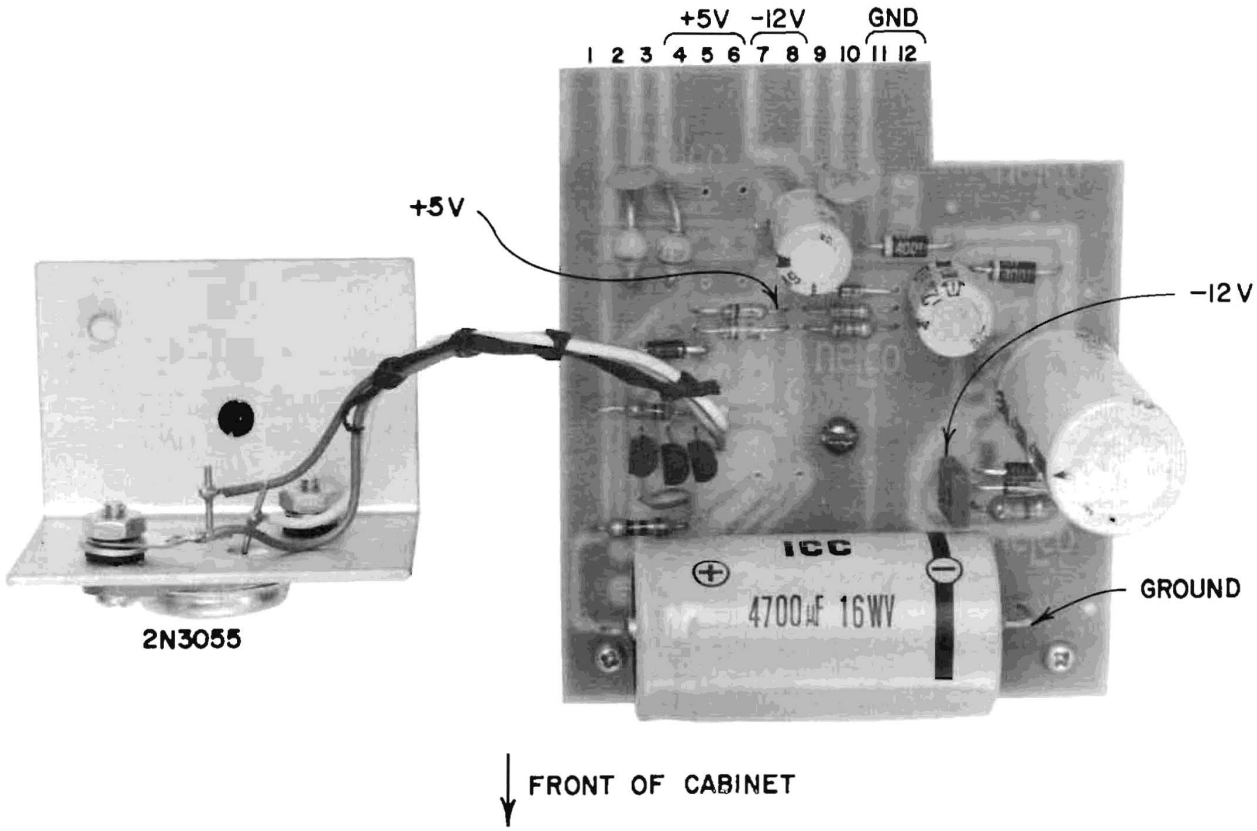


Figure 7.2 Power Supply (Serial No. less than 345)

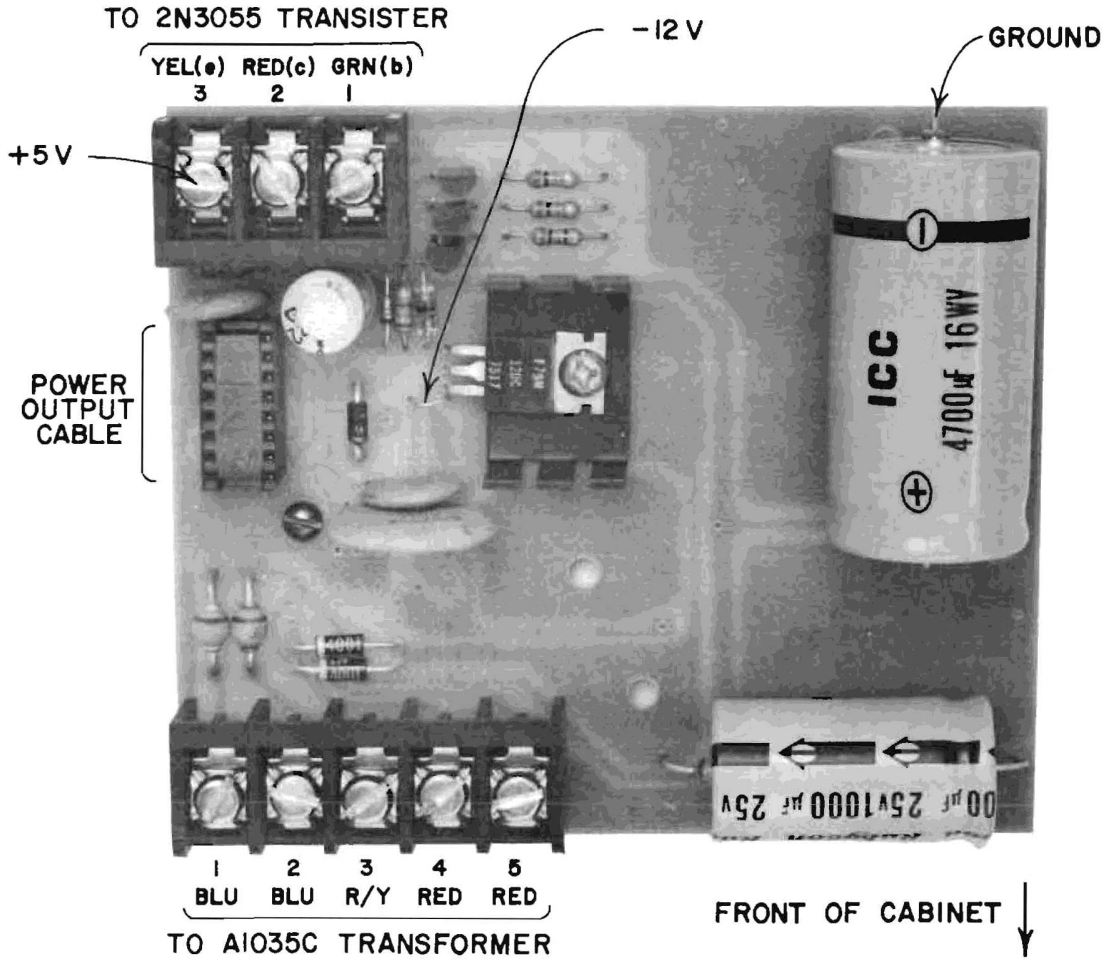


Figure 7.3 Power Supply (Serial No. 346 and higher)

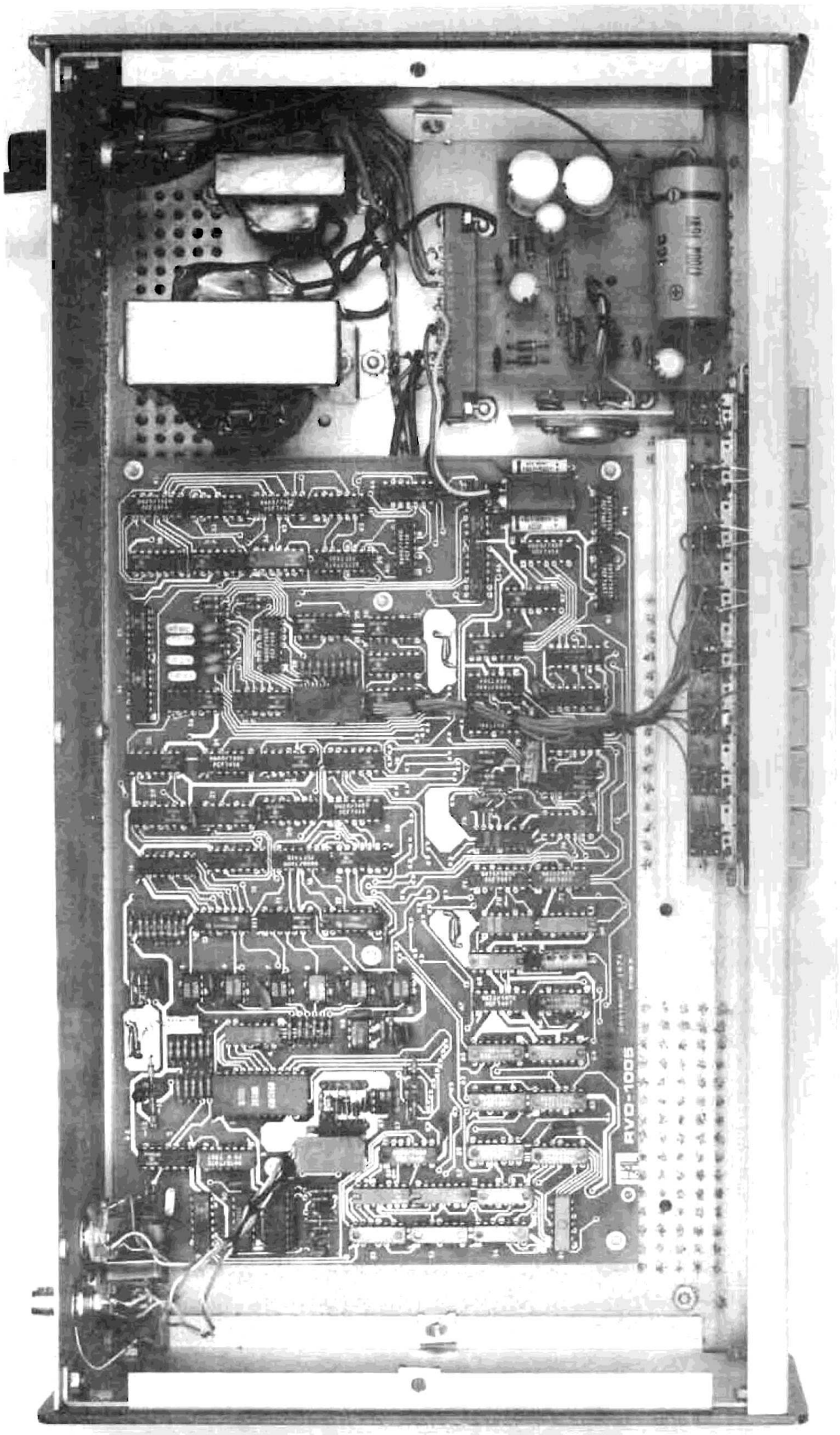


Figure 7.4 Interior of RVD (Serial No. less than 345)

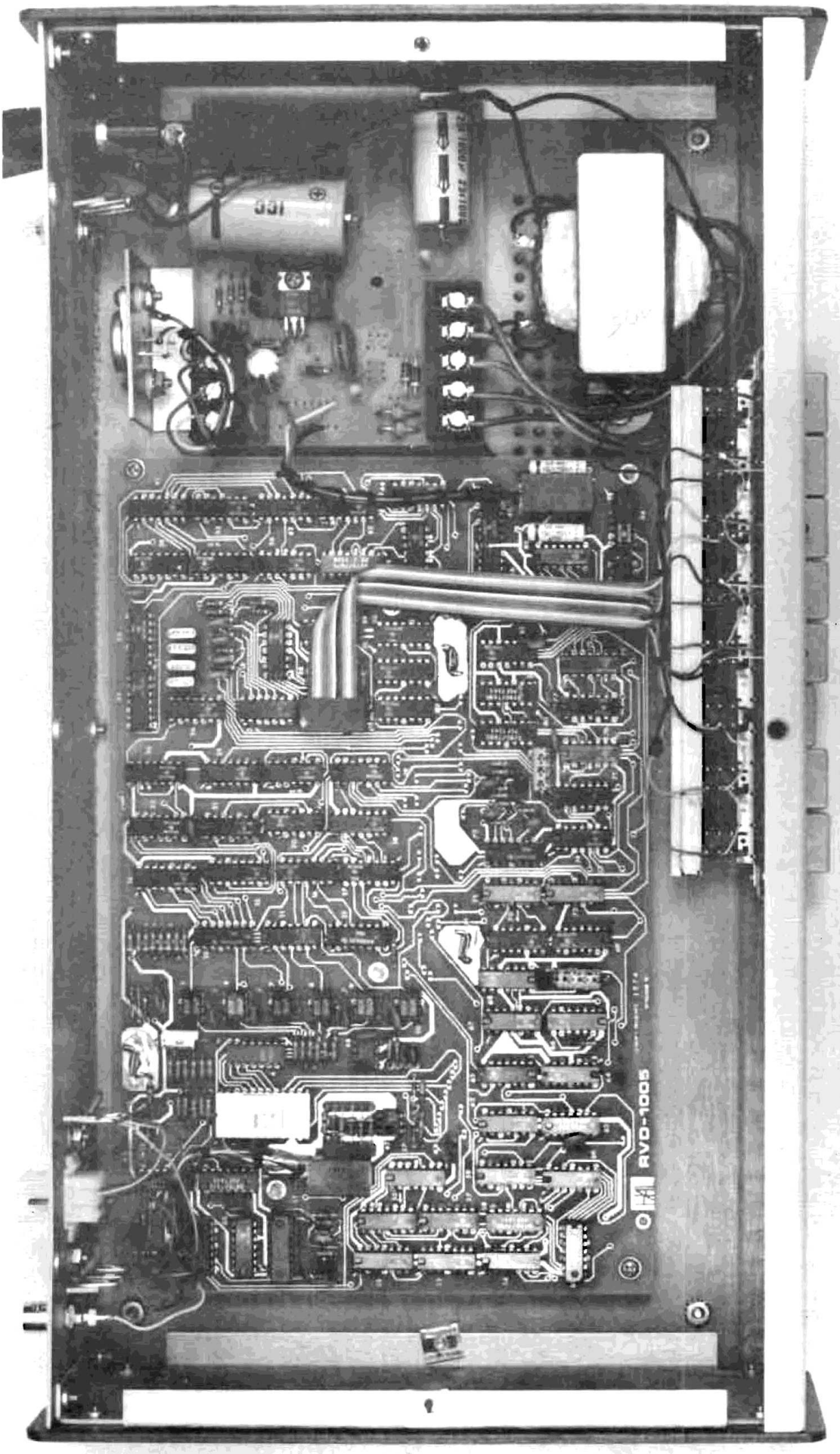


Figure 7.5 Interior of RVD (Serial No. 346 and higher)

8. Parts List

Integrated Circuits

1	FCD 810
1	2513N / CM9350
6	MM5013N (or 2525V)
1	MH0026CN
1	MM5320N
1	2519B
7	7400
1	7402
3	7404
1	7405
7	7410
7	7420
1	7430
1	7472
9	7473
9	7474
1	7475
2	7486
4	7490
2	7492
12	7493
1	7495
1	74123
2	74174
1	74188AN (red)
1	74188AN (blue)
1	74S04
1	79M12

Transistors

2	MPS3394
1	MPS3395
1	MPS3703
1	MU4892
5	MPS6518
1	2N3055

Diodes

1	1N270
2	1N4001
4	1N4005
7	1N4148
1	1N4731
1	1N4733
1	1N4735
1	1N4729
2	A15
5	RL4850 (LED)

Crystals

1	5957.81 kHz
1	6553.60 kHz
1	7459.98 kHz
1	9730.66 kHz
1	12272.7 kHz

Resistors

2	2.2 Ω, ¼ W
1	10 Ω, ¼ W
1	68 Ω, ¼ W
1	82 Ω, ¼ W
2	100 Ω, ¼ W
2	120 Ω, ¼ W
5	150 Ω, ¼ W
1	220 Ω, ¼ W
6	270 Ω, ¼ W
1	330 Ω, ¼ W
1	680 Ω, ¼ W
14	1.0 kΩ, ¼ W
1	1.2 kΩ, ¼ W
3	2.2 kΩ, ¼ W
1	2.7 kΩ, ¼ W
8	4.7 kΩ, ¼ W
12	6.8 kΩ. ¼ W
2	10 kΩ, ¼ W
6	22 kΩ, ¼ W
1	68 kΩ, ¼ W
1	100 kΩ, ¼ W

Capacitors

3	100 pF disc ceramic
4	220 pF disc ceramic
2	500 pF disc ceramic
8	.001 µF disc ceramic
12	.01 µF disc ceramic
3	.1 µF disc ceramic
1	2 µF electrolytic
1	10 µF electrolytic
1	25 µF electrolytic
2	50 µF electrolytic
1	220 µF electrolytic
1	1000 µF electrolytic
1	4700 µF electrolytic

Miscellaneous

1	D1106 Circuit Board
1	D1024 Circuit Board
3	16 DIP Sockets
1	14 DIP Socket
1	14 DIP Plug
1	16 DIP Plug
1	16 DIP Plug w. cable
1	UG1094 Connector
1	0309-2061 Connector
2	0309-1061 Connector
4	0209-2143 Male Pins
12	0209-1143 Female Pins
1	Video Cable w. connectors
3	3 lug terminal strips
1	3 lug barrier strip
1	5 lug barrier strip
1	6107B14 Heat Sink
1	Heat Sink for 2N3055
1	A1035 Power Transformer
1	8 Position PB Switch
1	Power Cord
1	HKP Fuse Holder
1	½ amp. SB Fuse
6	½" Plastic Stand-offs
2	6-32 × ½" Metal Spacers
1	Strain Relief
1	Cabinet with Hardware
1	RVD-1005 Manual